



GP
ELECTRONICS

GP18P07D33

18V P-Channel MOSFET

Product Summary

$V_{(BR)DSS}$	$R_{DS(on)TYP}$	I_D
-18V	5.6mΩ@-4.5V	-45A
	6.0mΩ@-3.7V	
	7.0mΩ@-2.5V	
	10.0mΩ@-1.8V	

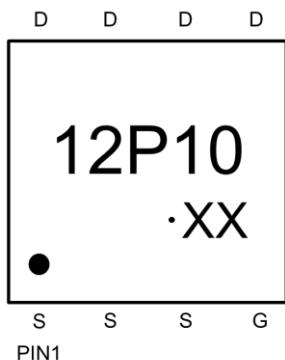
Feature

- High cell density trenched P-ch MOSFETs
- Super low gate charge
- Advanced high cell density Trench technology

Application

- Battery protection applications
- Load switch

MARKING:

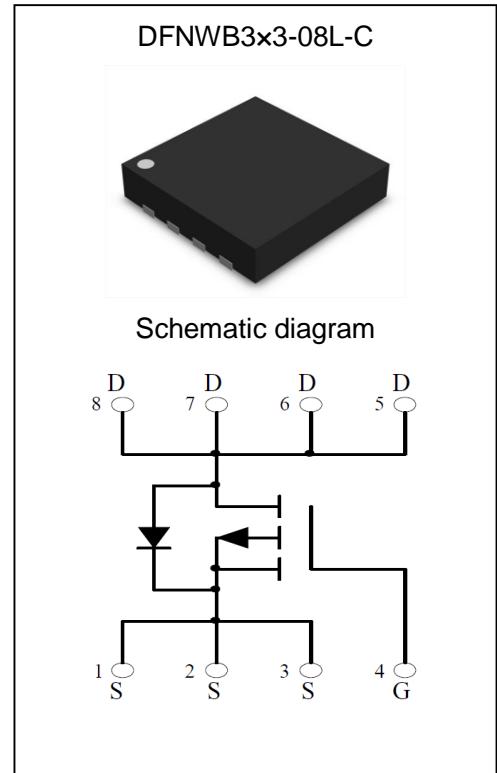


12P10 = Device code

Solid dot1 = Pin1 indicator

Solid dot2 = Green device, if none, normal device

XX = Date Code



ABSOLUTE MAXIMUM RATINGS ($T_a=25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	-18	V
Gate-Source Voltage	V_{GS}	± 8	V
Continuous Drain Current ¹	I_D	-45	A
Pulsed Drain Current ¹	I_{DM}	-135	A
Power Dissipation ²	P_D	3	W
Thermal Resistance from Junction to Ambient	$R_{\theta JA}$	42	°C/W
Junction Temperature	T_J	150	°C
Storage Temperature	T_{STG}	-55~+150	°C

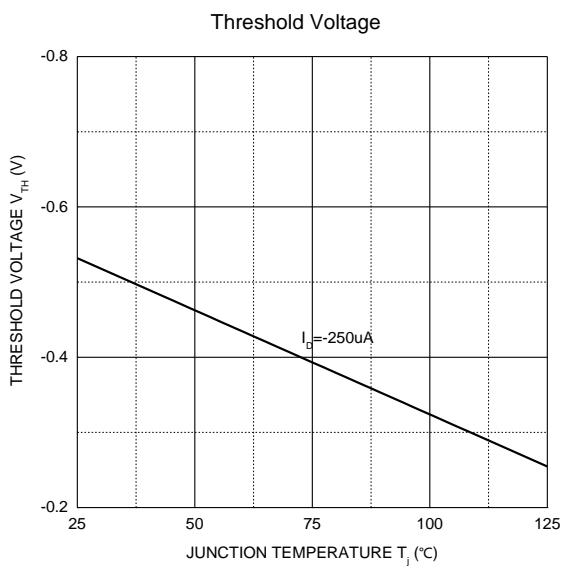
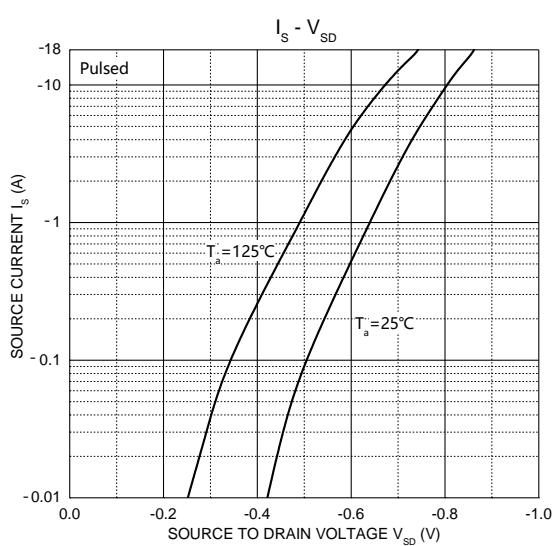
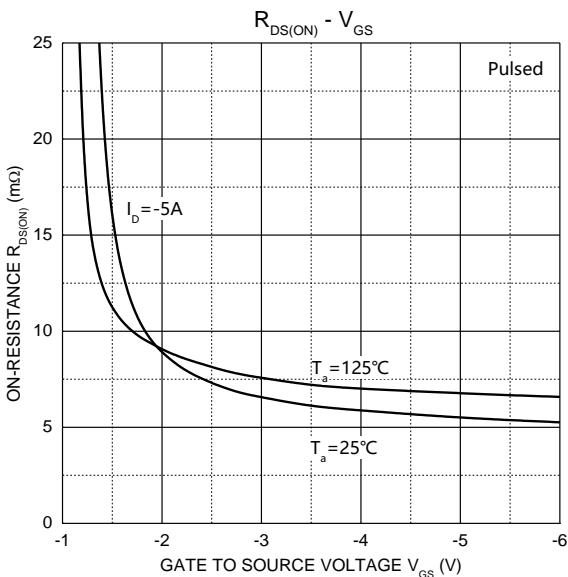
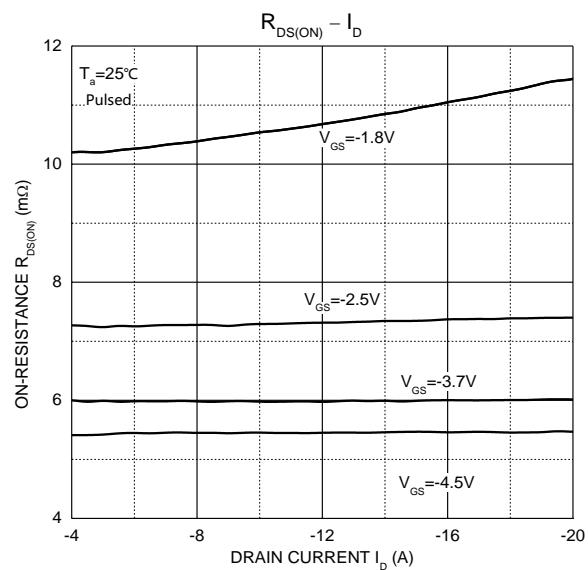
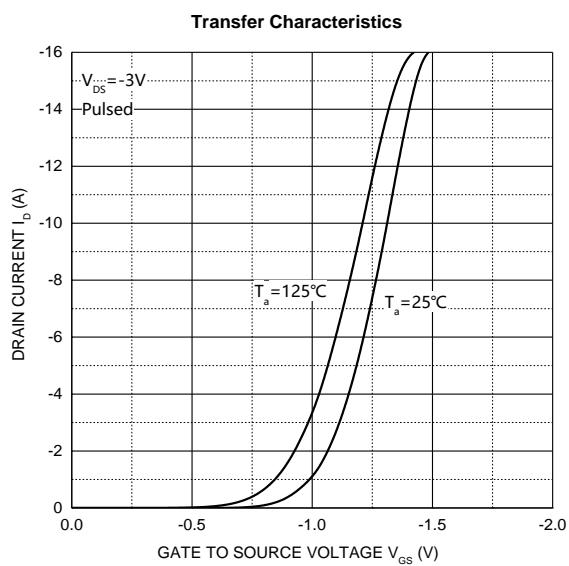
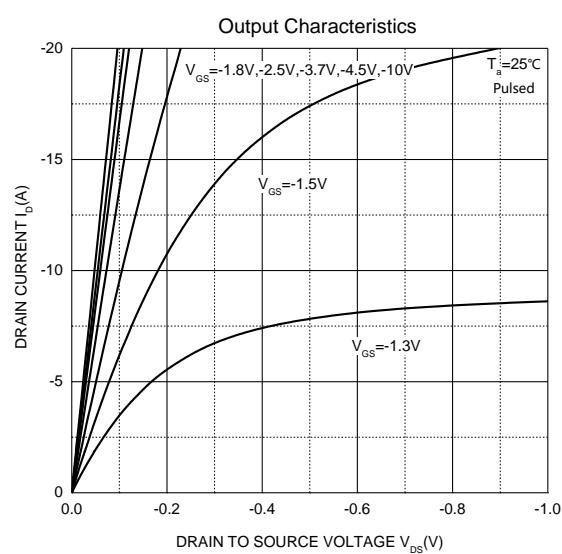
MOSFET ELECTRICAL CHARACTERISTICS($T_a=25^\circ\text{C}$ unless otherwise noted)

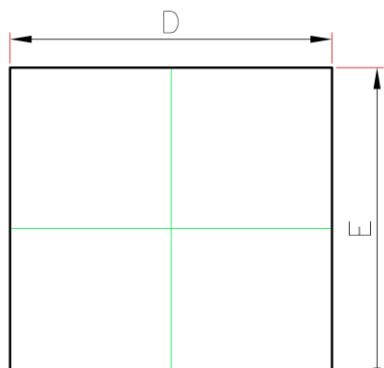
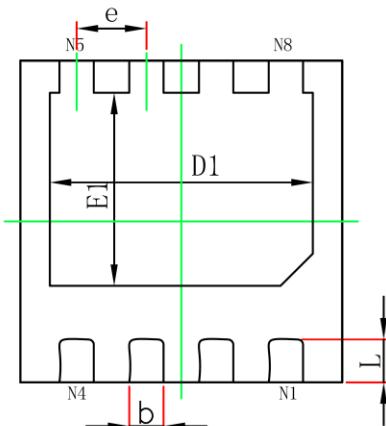
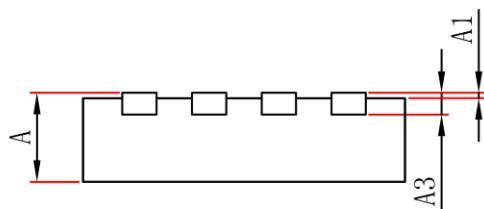
Parameter	Symbol	Test Condition	Min	Type	Max	Unit
Static Characteristics						
Drain-source breakdown voltage	$V_{(\text{BR})\text{DSS}}$	$V_{\text{GS}} = 0\text{V}, I_{\text{D}} = -250\mu\text{A}$	-18			V
Zero gate voltage drain current	I_{DSS}	$V_{\text{DS}} = -16\text{V}, V_{\text{GS}} = 0\text{V}$			-1	μA
Gate-body leakage current	I_{GSS}	$V_{\text{GS}} = \pm 8\text{V}, V_{\text{DS}} = 0\text{V}$			± 100	nA
Gate threshold voltage ³	$V_{\text{GS}(\text{th})}$	$V_{\text{DS}} = V_{\text{GS}}, I_{\text{D}} = -250\mu\text{A}$	-0.35	-0.5	-1	V
Drain-source on-resistance ³	$R_{\text{DS}(\text{on})}$	$V_{\text{GS}} = -4.5\text{V}, I_{\text{D}} = -10\text{A}$		5.6	7.3	mΩ
		$V_{\text{GS}} = -3.7\text{V}, I_{\text{D}} = -10\text{A}$		6.0	7.8	
		$V_{\text{GS}} = -2.5\text{V}, I_{\text{D}} = -8\text{A}$		7.0	9.4	
		$V_{\text{GS}} = -1.8\text{V}, I_{\text{D}} = -6\text{A}$		10	15	
Forward transconductance ³	g_{FS}	$V_{\text{DS}} = -6\text{V}, I_{\text{D}} = -10\text{A}$	5			S
Dynamic characteristics						
Input Capacitance	C_{iss}	$V_{\text{DS}} = -6\text{V}, V_{\text{GS}} = 0\text{V}, f = 1\text{MHz}$		4850		pF
Output Capacitance	C_{oss}			1520		
Reverse Transfer Capacitance	C_{rss}			1610		
Gate resistance	R_g	$f = 1\text{MHz}$			30	Ω
Total Gate Charge	Q_g	$V_{\text{DS}} = -6\text{V}, V_{\text{GS}} = -4.5\text{V}, I_{\text{D}} = -5\text{A}$		65		nC
Gate-Source Charge	Q_{gs}			20		
Gate-Drain Charge	Q_{gd}			325		
Turn-on delay time	$t_{\text{d}(\text{on})}$	$V_{\text{DD}} = -6\text{V}, V_{\text{GEN}} = -4.5\text{V}, I_{\text{D}} = -4\text{A}$ $R_L = 6\Omega, R_{\text{GEN}} = 1\Omega$		22		ns
Turn-on rise time	t_r			50		
Turn-off delay time	$t_{\text{d}(\text{off})}$			100		
Turn-off fall time	t_f			30		
Source-Drain Diode characteristics						
Diode forward current ⁴	I_s	$T_c = 25^\circ\text{C}$			-45	A
Diode pulsed forward current ⁴	I_{SM}				-135	A
Diode Forward voltage ³	V_{DS}	$V_{\text{GS}} = 0\text{V}, I_{\text{S}} = -10\text{A}$			-1.2	V

Notes:

- 1.Device mounted on FR-4 substrate board, with minimum recommended pad layout, single side.
- 2.The power dissipation is limited by 150°C junction temperature
- 3.Pulse Test : Pulse width $\leq 300\mu\text{s}$, duty cycle $\leq 2\%$.
- 4.The data is theoretically the same as I_{D} , in real applications , should be limited by total power dissipation.

Typical Electrical and Thermal Characteristics



DFNWB3x3-08L-C Package Information
DFNWB3×3-8L-C (P0. 65T0. 75) PACKAGE OUTLINE DIMENSIONS

TOP VIEW

BOTTOM VIEW

SIDE VIEW

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.203REF		0.008REF	
D	2.924	3.076	0.115	0.121
E	2.924	3.076	0.115	0.121
D1	2.350	2.550	0.093	0.100
E1	1.700	1.900	0.067	0.075
k	0.200MIN.		0.008MIN.	
b	0.270	0.370	0.011	0.015
e	0.650TYP.		0.026TYP.	
L	0.324	0.476	0.013	0.019