GPL6101 Series

Ultra Low Current Consumption 300mA CMOS Voltage Regulators

Product Summary

The GPL6101 series are a group of positive voltage regulators manufactured by CMOS technologies with ultra-low power consumption and low dropout voltage, which provide large output currents even when the difference of the input-output voltage is small. The GPL6101 series can deliver 300mA output current and allow an input voltage as high as 8V. The series are very suitable for the battery-powered equipments, such as RF applications and other systems requiring a quiet voltage source.

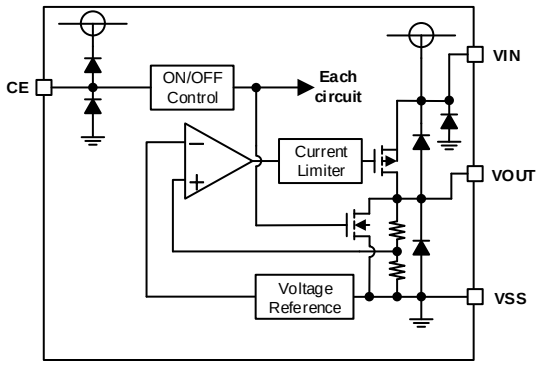
Features

- Low Quiescent Current: 0.8μA
- Operating Voltage Range: 1.8V～8V
- Output Current: 300mA
- Low Dropout Voltage: 110mV@100mA(VOUT=3.3V)
- Output Voltage: 1.2~5.0V
- High Accuracy: ±2%/±1%(Typ.)
- High Power Supply Rejection Ratio: 50dB@1kHz
- Low Output Noise: 27Xvout μV_{RMS}(10Hz~100kHz)
- Excellent Line and Load Transient Response
- Built-in Current Limiter, Short-Circuit Protection

Applications

- Portable consumer equipments
- Radio control systems
- Laptop, Palmtops and PDAs
- Wireless Communication Equipments
- Portable Audio Video Equipments
- Ultra-low Power Microcontroller

Block Diagram



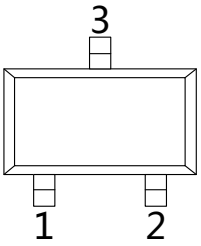
Order Information

GPL6101V①②

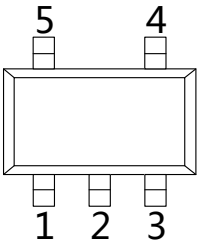
Designator	Description
①	Output Voltage e.g. 1.8V=18
②	Package: SOT-23-3L=K3 SOT-23-5L=K5 WBFBP-04C=H4 DFN1*1-4=H1 SOT-89-3L=KE

Pin Configuration

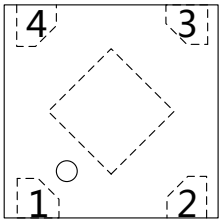
SOT-23-3



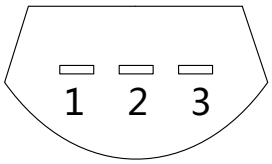
SOT-23-5



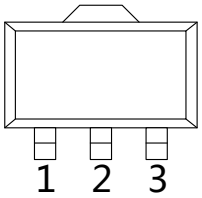
WBFBP-04C/DFN1*1-4L



TO-92



SOT-89-3



SOT-23-3L & TO-92 & SOT-89-3L

Pin Number			Pin Name	Function
SOT-23-3	TO-92	SOT-89-3L		
1	1	1	V_{SS}	Ground
2	3	3	V_{OUT}	Output
3	2	2	V_{IN}	Power input

SOT-23-5L

Pin Number	Pin Number	Function
1	V_{IN}	Power Input Pin
2	V_{SS}	Ground
3	CE	Chip Enable Pin
4	NC	No Connection
5	V_{OUT}	Output Pin

WBFBP-04C/DFN1*1-4L

Pin Number	Pin Number	Function
1	V_{OUT}	Output Pin
2	V_{SS}	Ground
3	CE	Chip Enable Pin
4	V_{IN}	Power Input Pin

Absolute Maximum Ratings[1] (T_a=25℃,unless otherwise noted)

Parameter		Symbol	Ratings	Units
Input Voltage[2]		V_{IN}	-0.3~9	V
Output Voltage[2]		V_{OUT}	-0.3~V_{IN}+0.3	V
Output Current		I_{OUT}	300	mA
Power Dissipation	SOT-23	P_D	0.4	W
	DFN1X1-4		0.4	W
	SOT-89		0.6	W
	TO-92		0.6	W
Operating Junction Temperature Range		T_j	-40~125	°C
Storage Temperature		T_{stg}	-40~125	°C
Lead Temperature(Soldering, 10 sec)		T_{solder}	260	°C

1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods my affect device reliability.

2) All voltages are with respect to network ground terminal.

Recommended Operating Conditions

Parameter	Min.	Nom.	Max.	Units
Supply voltage at V_{IN}	1.8		8	V
Operating junction temperature range, T_j	-40		125	°C
Operating free air temperature range, T_A	-40		85	°C

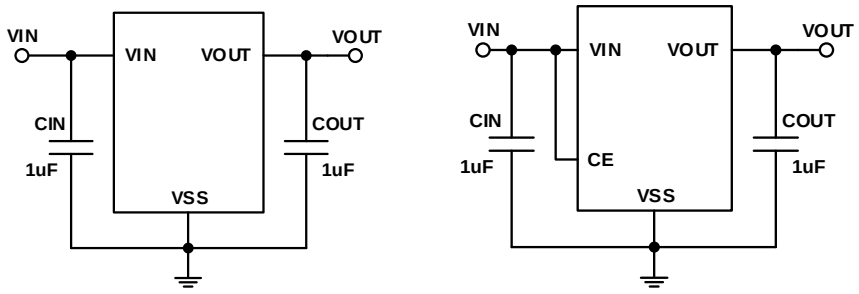
Electrical Characteristics (V_{IN}=V_{OUT}+1V, C_{IN}=C_{OUT}=1μF, T_A=25℃,unless otherwise specified)

Parameter	Symbol	Conditions		Min.	Typ.[3]	Max.	Units
Input Voltage	V_{IN}			1.8	—	8	V
Output Voltage Range	V_{OUT}			1.2	—	5	V
DC Output Accuracy		I_{OUT}=1mA		-2	—	2	%
				-1	—	1	%
Dropout Voltage	V_{dif}[4]	I_{OUT} =100mA,V_{OUT}=3.3V		—	110	—	mV
Supply Current	I_{SS}	I_{OUT}=0	1.2V≤V_{OUT}≤3.3V	—	0.8	1.3	μA
			3.3V<V_{OUT}≤5.0V		1.0	1.5	μA
Standby Current	I_{STBY}	CE=V_{SS}				0.1	μA
Line Regulation	$\frac{\Delta V_{OUT}}{V_{OUT} \times \Delta V_{IN}}$	I_{OUT} =10mA V_{OUT} +1V≤V_{IN}≤8V		—	0.05	0.3	%/V
Load Regulation	ΔV_{OUT}	V_{IN}= V_{OUT} +1V, 1mA≤I_{OUT}≤100mA		—	10	—	mV
Temperature Coefficient	$\frac{\Delta V_{OUT}}{V_{OUT} \times \Delta T_A}$	I_{OUT}=10mA, -40°C<T_A<125°C			100		ppm
Output Current Limit	I_{LIM}	V_{OUT}= 0.5 x $V_{OUT(Normal)}$, V_{IN} = 5V		550	700	850	mA
Short Current	I_{SHORT}	V_{OUT} =V_{SS}		—	20	—	mA
Power Supply Rejection Ratio	PSRR	I_{OUT}=50mA	100Hz		70		dB
			1kHz	—	50	—	
			10kHz	—	40	—	
			100kHz	—	35	—	
Output Noise Voltage	V_{ON}	BW=10Hz to 100kHz		—	27 x V_{OUT}	—	μV_{RMS}
CE "High" Voltage	V_{CE}"H"			1.5		V_{IN}	V
CE "Low" Voltage	V_{CE}"L"					0.3	V
C_{OUT} Auto-Discharge Resistance	$R_{DISCHRG}$	V_{IN}=5V, V_{OUT}=3.0V, V_{CE}=V_{SS}			200		Ω

3) Typical numbers are at 25°C and represent the most likely norm.

4) V_{dif}: The Difference Of Output Voltage And Input Voltage When Input Voltage Is Decreased Gradually Till Output Voltage Equals To 98% Of V_{OUT} (E).

Typical Application



Application Information

Selection of Input/ Output Capacitors

In general, all the capacitors need to be low leakage. Any leakage the capacitors have will reduce efficiency, increase the quiescent current.

A recent trend in the design of portable devices has been to use ceramic capacitors to filter DC-DC converter inputs. Ceramic capacitors are often chosen because of their small size, low equivalent series resistance (ESR) and high RMS current capability. Also, recently, designers have been looking to ceramic capacitors due to shortages of tantalum capacitors.

Unfortunately, using ceramic capacitors for input filtering can cause problems. Applying a voltage step to a ceramic capacitor causes a large current surge that stores energy in the inductances of the power leads. A large voltage spike is created when the stored energy is transferred from these inductances into the ceramic capacitor. These voltage spikes can easily be twice the amplitude of the input voltage step.

Many types of capacitors can be used for input bypassing, however, caution must be exercised when using multilayer ceramic capacitors (MLCC). Because of the self-resonant and high Q characteristics of some types of ceramic capacitors, high voltage transients can be generated under some start-up conditions, such as connecting the LDO input to a live power source. Adding a 3Ω resistor in series with an X5R ceramic capacitor will minimize start-up voltage transients.

The LDO also requires an output capacitor for loop stability. Connect a 1μF tantalum capacitor from OUT to GND close to the pins. For improved transient response, this output capacitor may be ceramic.

C_{OUT} Auto-Discharge Function

YP5108B series can discharge the electric charge in the output capacitor (C_{OUT}), when a low signal to the CE pin, which enables a whole IC circuit turn off, is inputted via the N-channel transistor located between the V_{OUT} pin and the V_{SS} pin (cf. BLOCK DIAGRAM). The C_{OUT} auto-discharge resistance value is set at 200Ω (V_{OUT}=3.0V @ V_{IN}=5.0V at typical). The discharge time of the output capacitor (C_{OUT}) is set by the C_{OUT} auto-discharge resistance (R) and the output capacitor (C_{OUT}). By setting time constant of a C_{OUT} auto-discharge resistance value [$R_{DISCHRG}$] and an output capacitor value (C_{OUT}) as τ (τ=C x $R_{DISCHRG}$), the output voltage after discharge via the N-channel transistor is calculated by the following formulas.

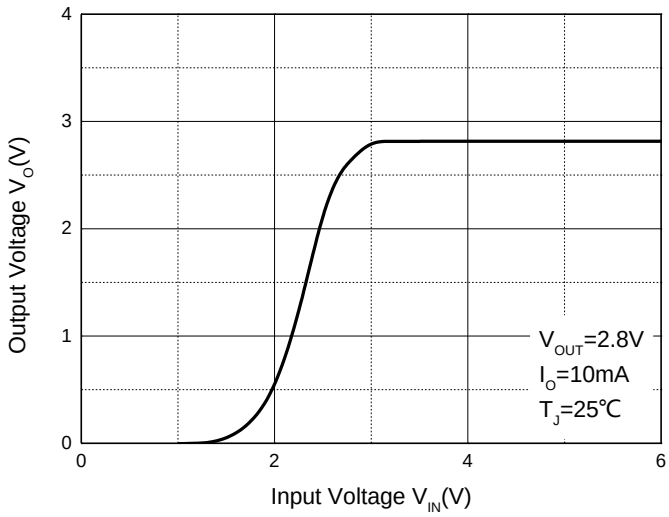
$$V = VOUT(E) \times e^{-t/\tau}, \text{or } t = \tau \ln(V/VOUT(E))$$

(V : Output voltage after discharge, $V_{OUT(E)}$: Output voltage, t: Discharge time,

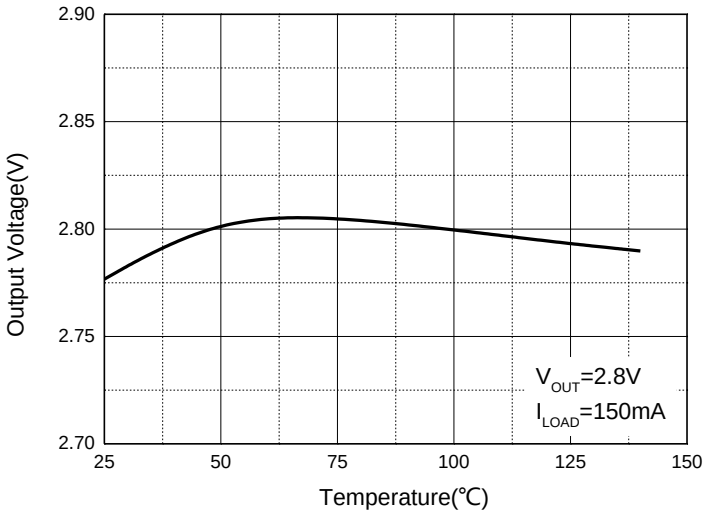
τ: C_{OUT} auto-discharge resistance $R_{DISCHRG}$×Output capacitor (C_{OUT}) value C)

Typical Performance Characteristics

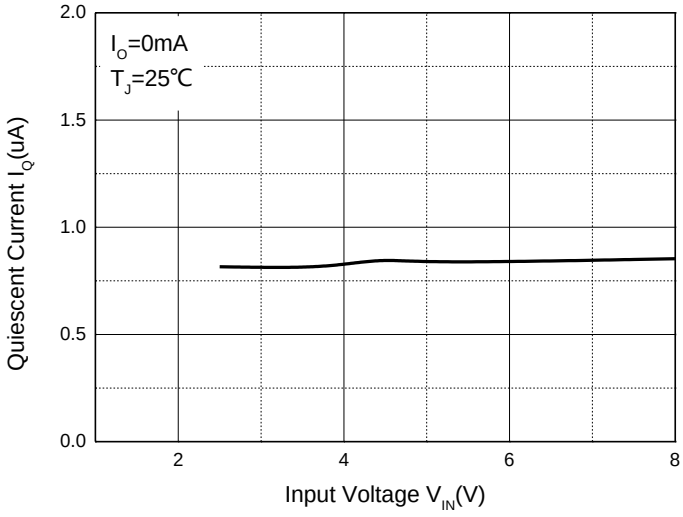
Output Characteristics



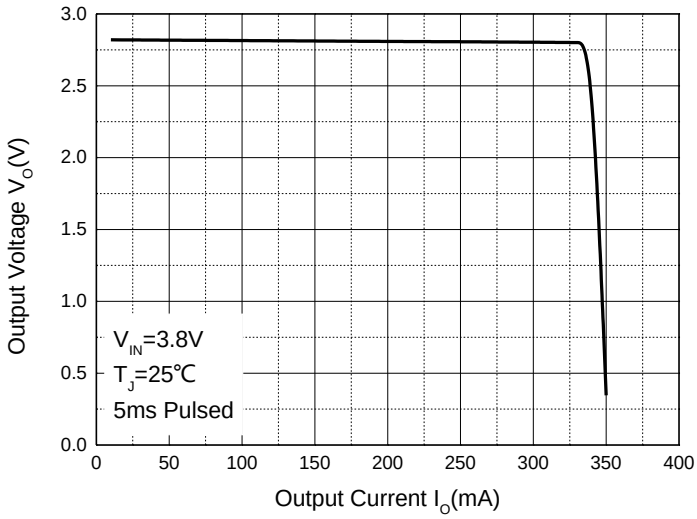
Output Voltage vs. Temperature



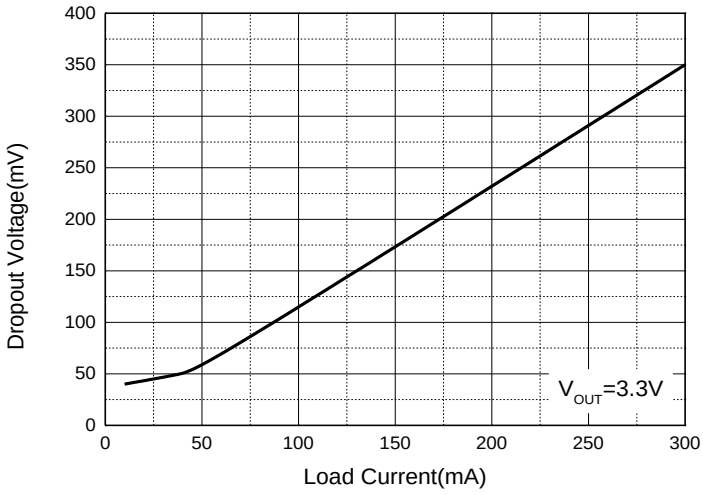
Quiescent Current



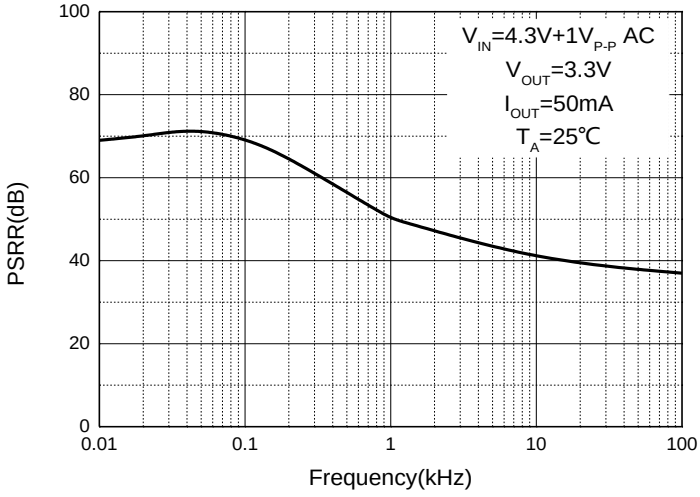
Current Cut-off Grid Voltage



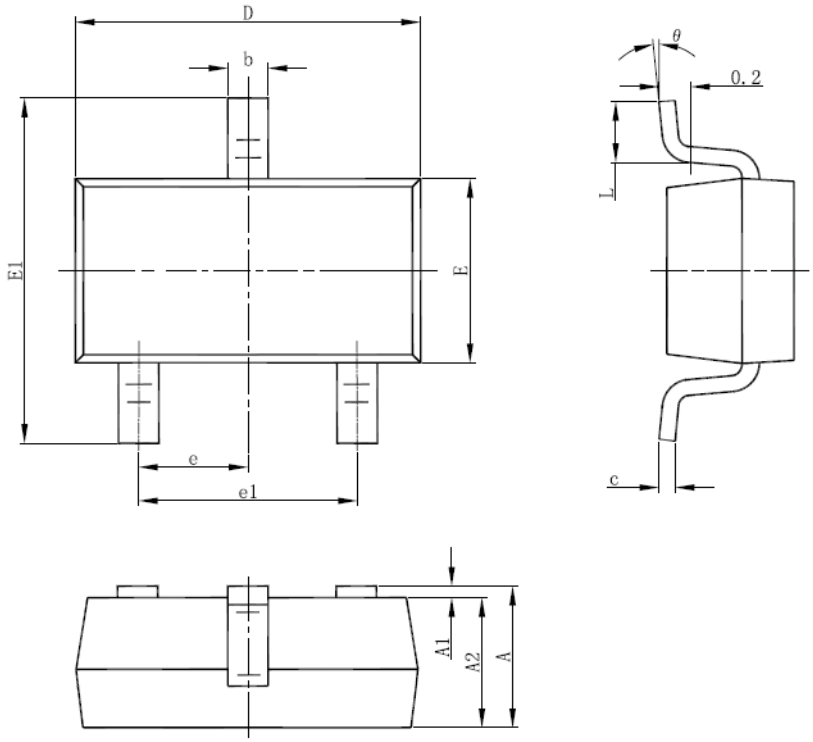
Dropout Voltage vs. Load Current



PSRR vs. Frequenc

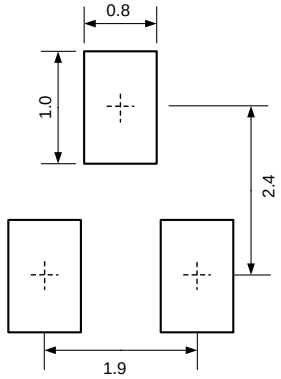


SOT-23-3L Package Outline Dimensions



Symbol	Dimensions in millimeters	
	Min.	Max.
A	1.050	1.250
A1	0.000	0.100
A2	1.050	1.150
b	0.300	0.500
c	0.100	0.200
D	2.820	3.020
E	1.500	1.700
E1	2.650	2.950
e	0.950TYP	
e1	1.800	2.000
L	0.300	0.600
θ	0°	8°

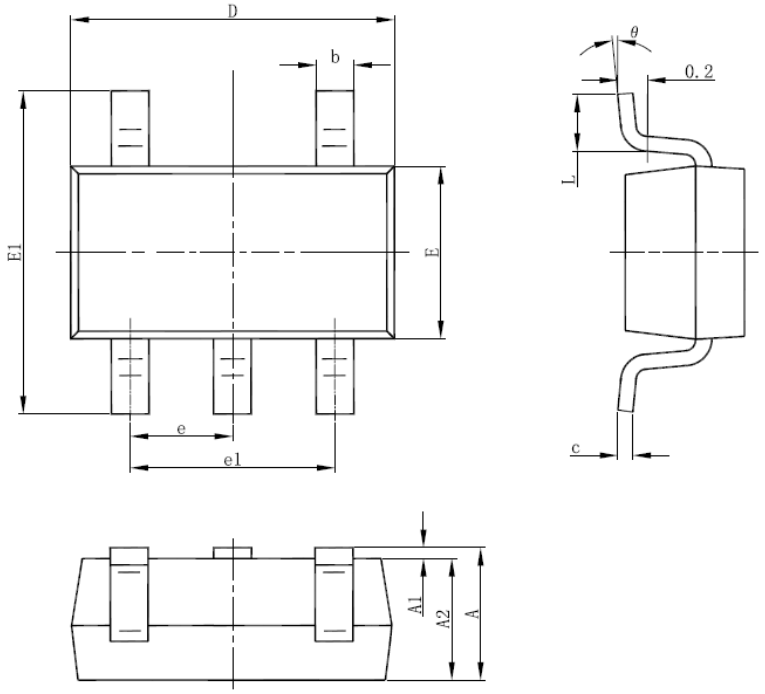
SOT-23-3L Suggested Pad Layout (Unit: mm)



Notes:

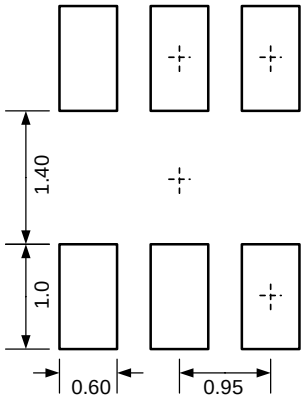
1. General tolerance:±0.05mm.
2. The pad layout is for reference purposes only.

SOT-23-5L Package Outline Dimensions



Symbol	Dimensions In Millimeters	
	Min.	Max.
A	1.050	1.250
A1	0.000	0.100
A2	1.050	1.150
b	0.300	0.500
c	0.100	0.200
D	2.820	3.020
E	1.500	1.700
E1	2.650	2.950
e	0.950(BSC)	
e1	1.800	2.000
L	0.300	0.600
θ	0°	8°

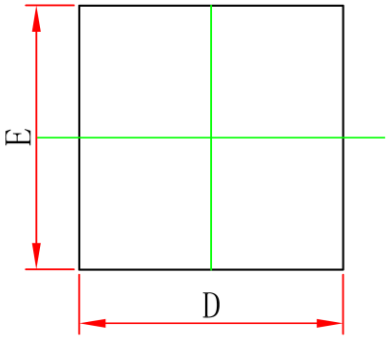
SOT-23-5L Suggested Pad Layout (Unit: mm)



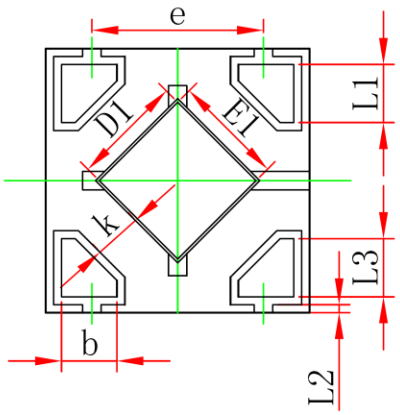
Notes:

1. General tolerance:±0.05mm.
2. The pad layout is for reference purposes only.

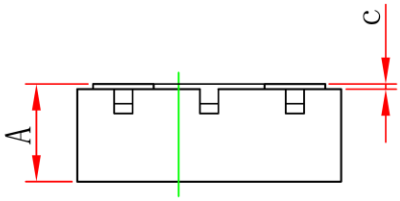
WBFBP-04C Package Outline Dimensions



TOP VIEW
[顶视图]



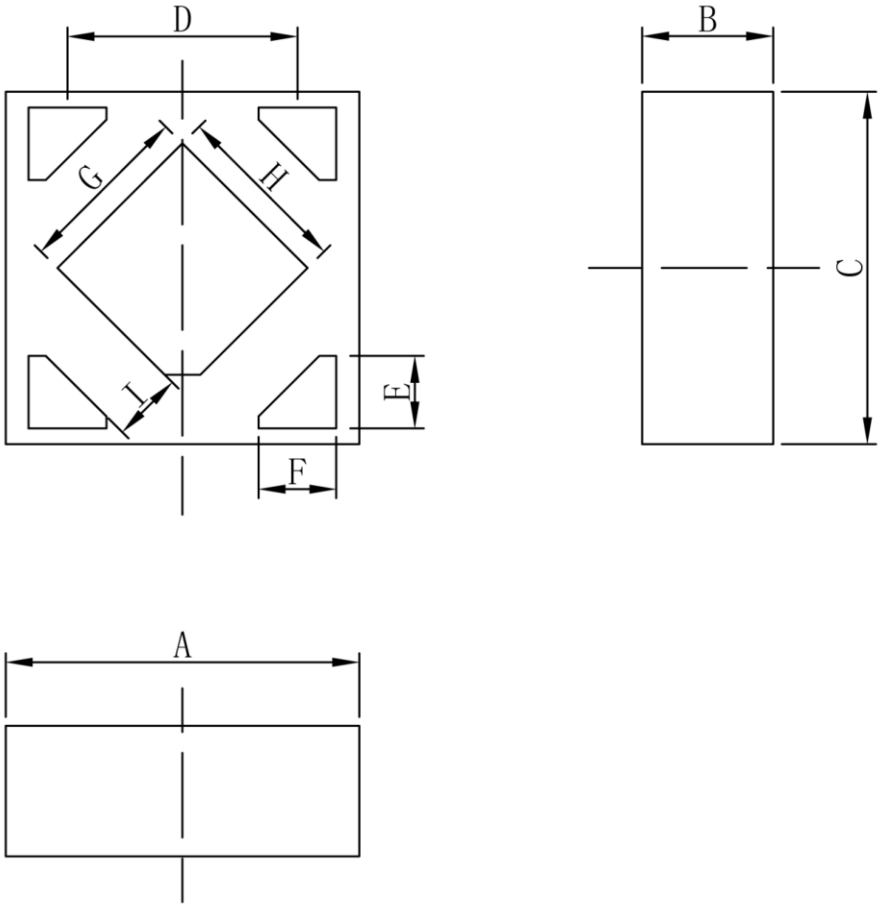
BOTTOM VIEW
[背视图]



SIDE VIEW
[侧视图]

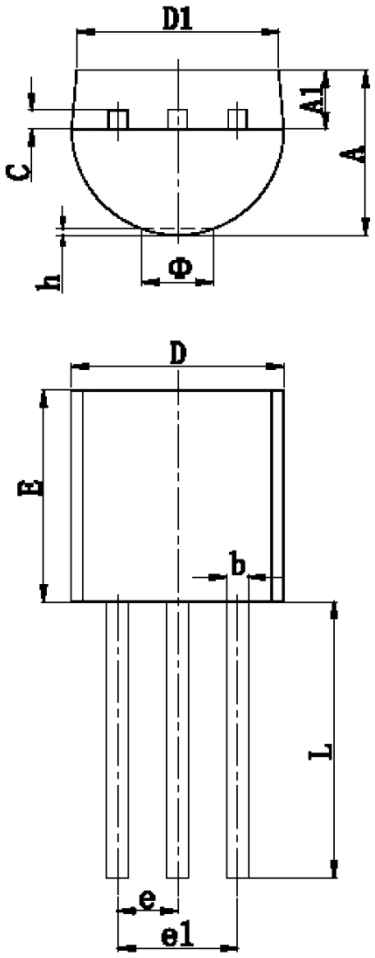
Symbol	Dimensions in millimeters		Dimensions in inches	
	Min.	Max.	Min.	Max.
A	0.335	0.495	0.013	0.016
D	0.950	1.050	0.037	0.041
E	0.950	1.050	0.037	0.041
D1	0.037	0.047	0.015	0.019
E1	0.037	0.047	0.015	0.019
k	0.17MIN		0.007MIN	
b	0.160	0.260	0.006	0.010
c	0.010	0.090	0.000	0.004
e	0.600	0.700	0.024	0.028
L1	0.185	0.255	0.007	0.010
L2	0.030REF		0.001REF	
L3	0.185	0.255	0.007	0.010

DFN1*1-4L Package Outline Dimensions



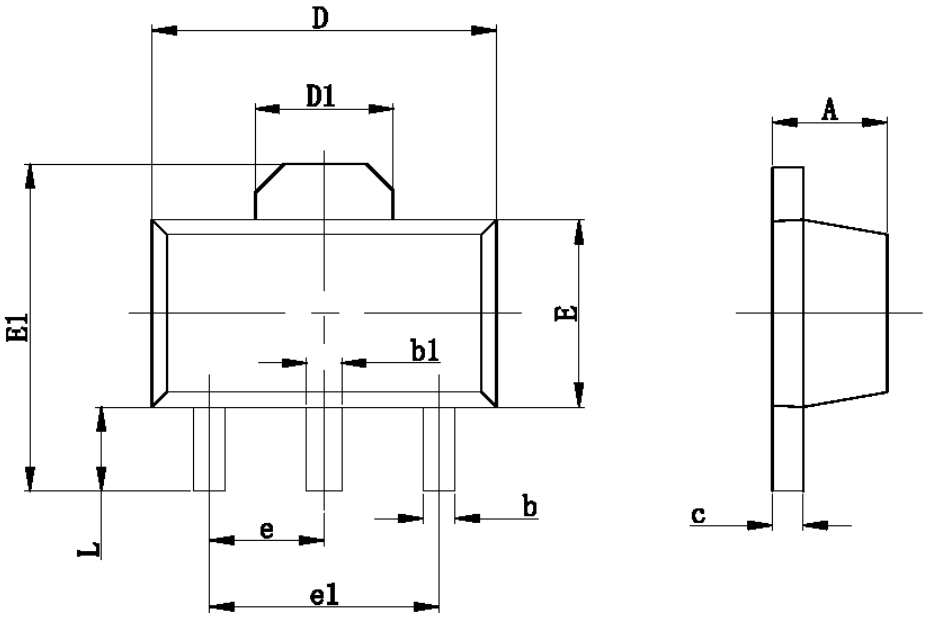
Symbol	Dimensions in millimeters	
	Min.	Max.
A	0.950	1.050
B	0.320	0.420
C	0.950	1.050
D	0.600	0.700
E	0.175	0.275
F	0.170	0.270
G	0.440	0.540
H	0.440	0.540
I	0.140	0.240

TO-92 Package Outline Dimensions



Symbol	Dimensions in millimeters		Dimensions in inches	
	Min.	Max.	Min.	Max.
A	3.300	3.700	0.130	0.146
A1	1.100	1.400	0.043	0.055
b	0.380	0.550	0.015	0.022
c	0.360	0.510	0.014	0.020
D	4.400	4.700	0.173	0.185
D1	3.430		0.135	
E	4.300	4.700	0.169	0.185
e	1.270TYP		0.050TYP	
e1	2.440	2.640	0.096	0.104
L	14.100	14.500	0.555	0.571
ϕ		1.600		0.063
h	0.000	0.380	0.000	0.015

SOT-89-3L Package Outline Dimensions



Symbol	Dimensions in millimeters		Dimensions in inches	
	Min.	Max.	Min.	Max.
A	1.400	1.600	0.055	0.063
b	0.320	0.520	0.013	0.197
b1	0.400	0.580	0.016	0.023
c	0.350	0.440	0.014	0.017
D	4.400	4.600	0.173	0.181
D1	1.550REF		0.061REF	
E	2.300	2.600	0.091	0.102
E1	3.940	4.250	0.155	0.167
e	1.500TYP		0.060TYP	
e1	3.000TYP		0.118TYP	
L	0.900	1.200	0.035	0.047