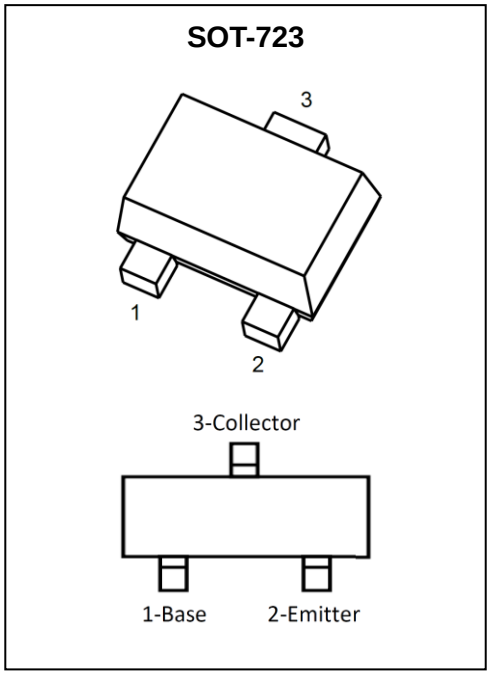
DTC114TM

Digital Transistor

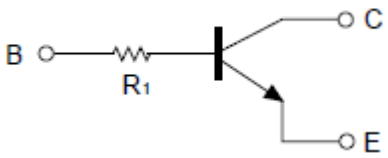
DTC114TM Digital Transistor(NPN)



Feature

- Built-in bias resistors enable the configuration of an inverter circuit without connecting external input resistors
- The bias resistors consist of thin-film resistors with complete isolation to allow positive biasing of the input .They also have the advantage of almost completely eliminating parasitic effects
- Only the on/off conditions need to be set for operation, making device design easy

Schematic diagram



ABSOLUTE MAXIMUM RATINGS (T_a=25℃ unless otherwise noted)

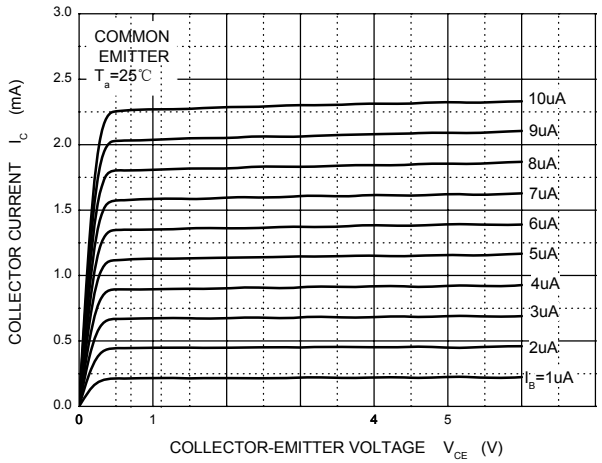
Parameter	Symbol	Value	Unit
Collector-base Voltage	V_{CBO}	50	V
Collector-emitter Voltage	V_{CEO}	50	V
Collector current	I_C	100	mA
Power Dissipation	P_D	100	mW
Junction Temperature	T_J	125	℃
Storage Temperature Range	T_{STG}	-45 ~ +125	℃

ELECTRICAL CHARACTERISTICS (T_a=25℃ unless otherwise noted)

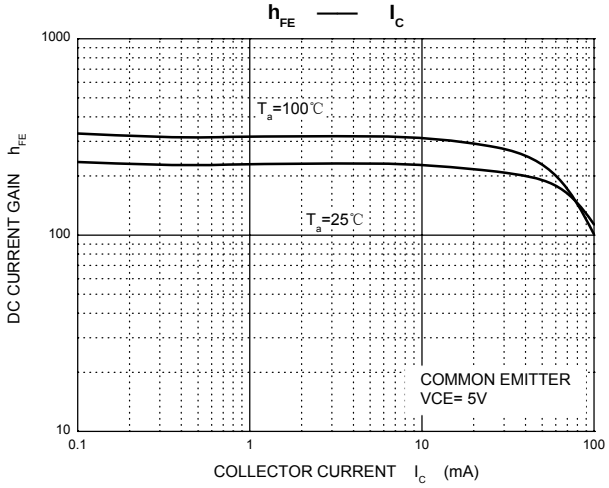
Parameter	Symbol	Test Condition	Min	Type	Max	Unit
Collector-base breakdown voltage	BV_{CBO}	I_C=50μA	50			V
Collector-emitter breakdown	BV_{CEO}	I_C=1mA	50			V
Emitter-base breakdown voltage	BV_{EBO}	I_E=50μA	5			V
Collector cutoff current	I_{CBO}	V_{CB}=50V			0.5	μA
Emitter cutoff current	I_{EBO}	V_{EB}=4V			0.5	μA
Collector-emitter saturation	$V_{CE(SAT)}$	I_C=10mA ,I_B=1mA			0.3	V
DC current transfer ratio	h_{FE}	I_C=1mA,V_{CE}=5V	100		600	
Input resistance	R_1		7	10	13	kΩ
Transition frequency	f_T	V_{CE}=10V,I_E=5mA,f=1MHz		250		MHz

Typical Characteristics

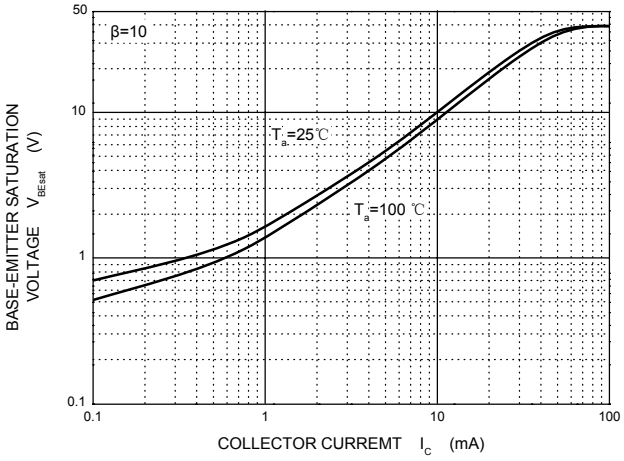
Static Characteristic



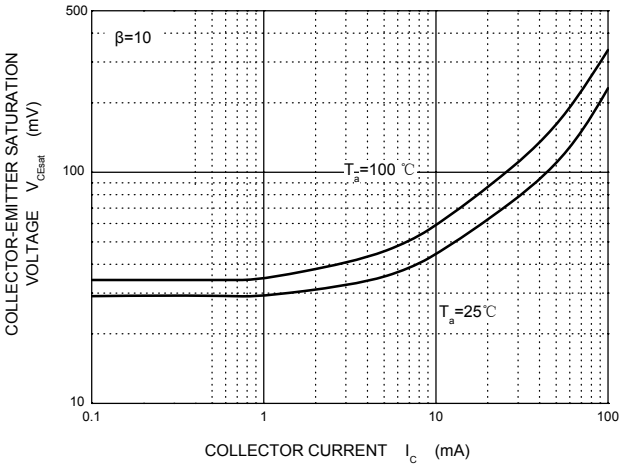
h_{FE} —— I_C



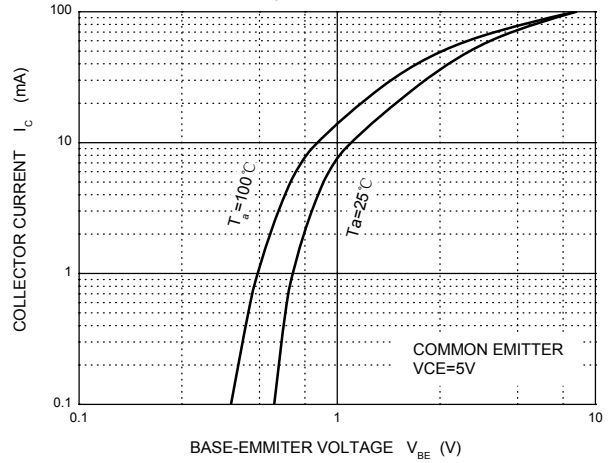
V_{BEsat} —— I_C



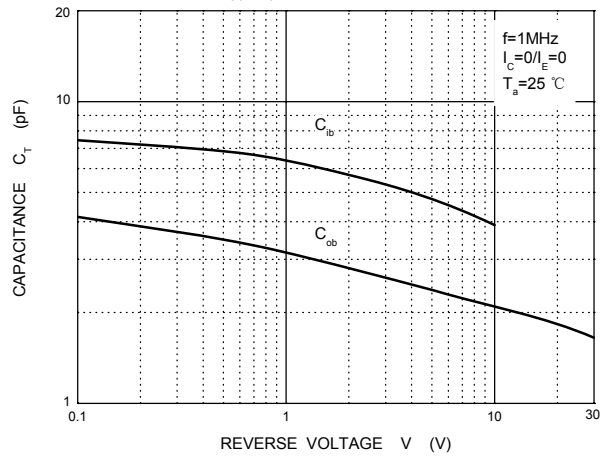
V_{CEsat} —— I_C



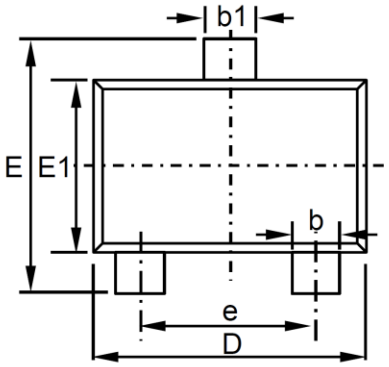
I_C —— V_{BE}

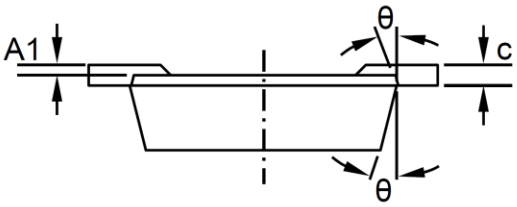


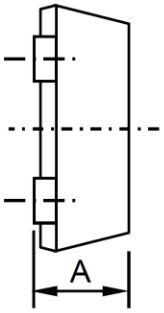
C_{ob}/C_{ib} —— V_{CB}/V_{EB}



SOT-723 Package Information

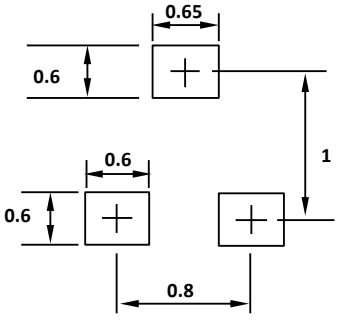






SOT-723 （unit：mm）		
Dim.	Min.	Max.
A	0.40	0.50
A1	0.00	0.05
b	0.15	0.27
b1	0.20	0.37
c	0.06	0.16
D	1.10	1.30
E	1.10	1.30
E1	0.70	0.90
e	0.80 TYP.	
θ	7° REF.	

SOT-723 Suggested Pad Layout



Note:
1.Controlling dimension:in millimeters.
2.General tolerance:± 0.05mm.
3.The pad layout is for reference purposes only.