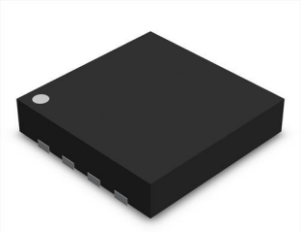
GP12P12D33

12V P-Channel MOSFET

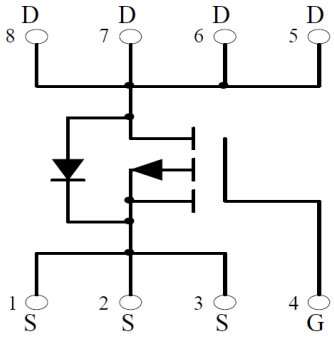
Product Summary

$V_{(BR)DSS}$	$R_{DS(on)TYP}$	I_D
-12V	8mΩ@-4.5V	-27A
	9mΩ@-3.7V	
	10mΩ@-2.5V	
	15mΩ@-1.8V	

DFN3×3-8L



Schematic diagram



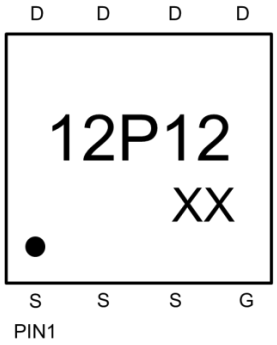
Feature

- High cell density trenched P-ch MOSFETs
- Super low gate charge
- Advanced high cell density Trench technology

Application

- Battery protection applications
- Load switch

MARKING:



12P12= Device code

Solid dot=Pin1 indicator

XX=Date Code

ABSOLUTE MAXIMUM RATINGS (T_a=25℃ unless otherwise noted)

Parameter	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	-12	V
Gate-Source Voltage	V_{GS}	±10	V
Continuous Drain Current[1]	I_D	-27	A
Pulsed Drain Current[1]	I_{DM}	-81	A
Power Dissipation[2]	P_D	3	W
Thermal Resistance from Junction to Ambient	$R_{\theta JA}$	42	℃/W
Junction Temperature	T_J	150	℃
Storage Temperature	T_{STG}	-55~ +150	℃

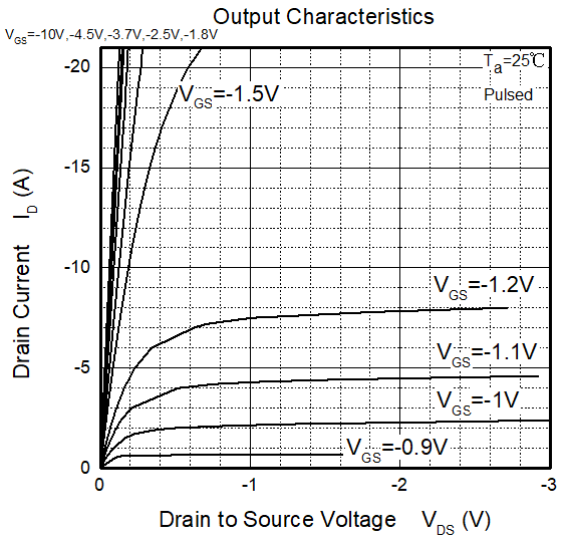
MOSFET ELECTRICAL CHARACTERISTICS(T_a=25℃ unless otherwise noted)

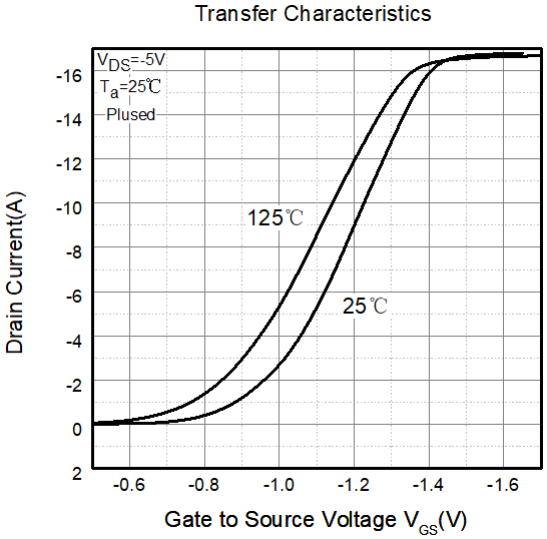
Parameter	Symbol	Test Condition	Min	Type	Max	Unit
Static Characteristics						
Drain-source breakdown voltage	$V_{(BR)DSS}$	V_{GS} = 0V, I_D =-250μA	-12	-19	-20	V
Zero gate voltage drain current	I_{DSS}	V_{DS} =-12V,V_{GS} = 0V			-1	μA
Gate-body leakage current	I_{GSS}	V_{GS} =±12V, V_{DS} = 0V			±100	nA
Gate threshold voltage[3]	$V_{GS(th)}$	V_{DS} =V_{GS}, I_D =-250μA	-0.4	-0.7	-1.0	V
Drain-source on-resistance[3]	$R_{DS(on)}$	V_{GS} =-4.5V, I_D =-10A		8	12	mΩ
		V_{GS} =-3.7V, I_D =-10A		9	13	
		V_{GS} =-2.5V, I_D =-8A		10	14	
		V_{GS} =-1.8V, I_D =-6A		15	19	
Forward tranconductance[3]	g_{FS}	V_{DS} =-5V, I_D =-10A	5			S
Dynamic characteristics[4]						
Input Capacitance	C_{iss}	V_{DS} =-6V,V_{GS} =0V,f =1MHz		3850		pF
Output Capacitance	C_{oss}			970		
Reverse Transfer Capacitance	C_{rss}			1000		
Gate resistance	R_g	f =1MHz			15	Ω
Total Gate Charge	Q_g	V_{DS} =-6V,V_{GS} =-4.5V,I_D=-5A		42		nC
Gate-Source Charge	Q_{gs}			6.9		
Gate-Drain Charge	Q_{gd}			10.8		
Turn-on delay time	$t_{d(on)}$	V_{DD}=-6V,V_{GEN}=-4.5V,I_D=-4A R_L=6Ω,R_{GEN}=1Ω		20		Ns
Turn-on rise time	t_r			15		
Turn-off delay time	$t_{d(off)}$			45		
Turn-off fall time	t_f			22		
Source-Drain Diode characteristics						
Diode forward current[5]	I_S	T_C=25℃			-27	A
Diode pulsed forward curren[5]	I_{SM}				-80	A
Diode Forward voltage[3]	V_{DS}	V_{GS} =0V, I_S=-10A		-0.8	-1.2	V

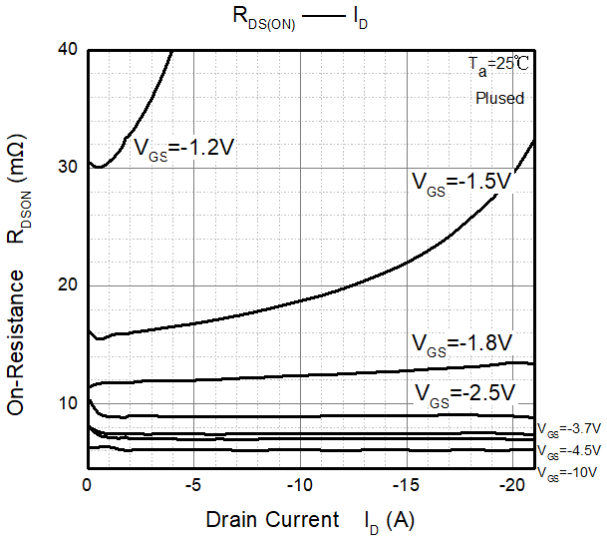
Notes:

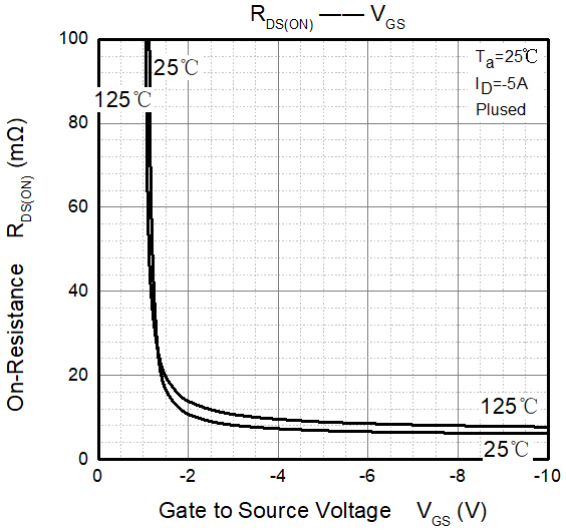
1. Device mounted on FR-4 substrate board, with minimum recommended pad layout, single side.
2. The power dissipation is limited by 150℃ junction temperature
3. Pulse Test : Pulse width≤300μs, duty cycle≤2%.
4. Guaranteed by design, not subject to production testing.
5. The data is theoretically the same as I_D, in real applications , should be limited by total power dissipation.

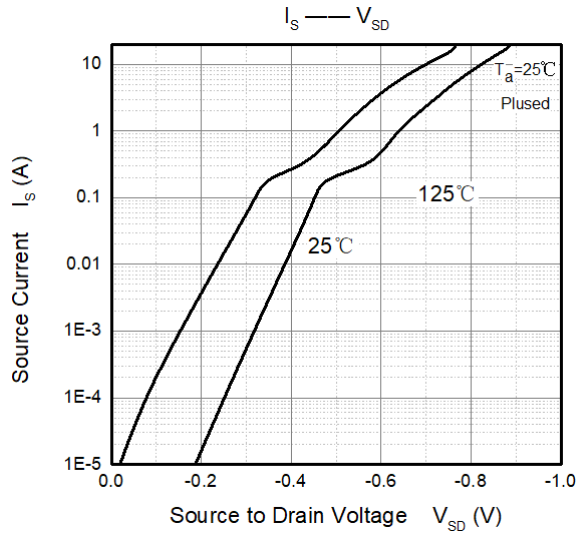
Typical Electrical and Thermal Characteristics

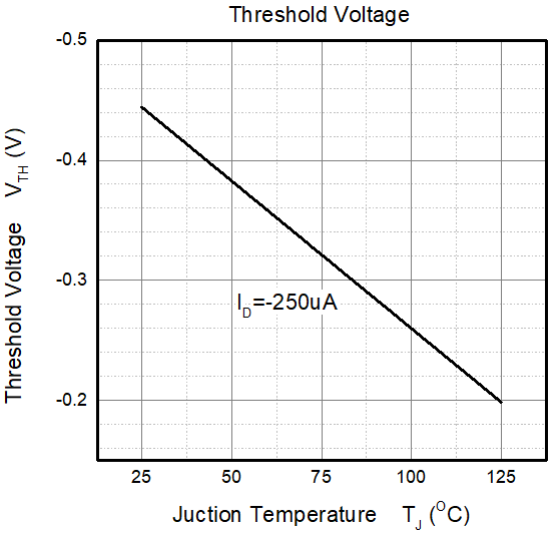




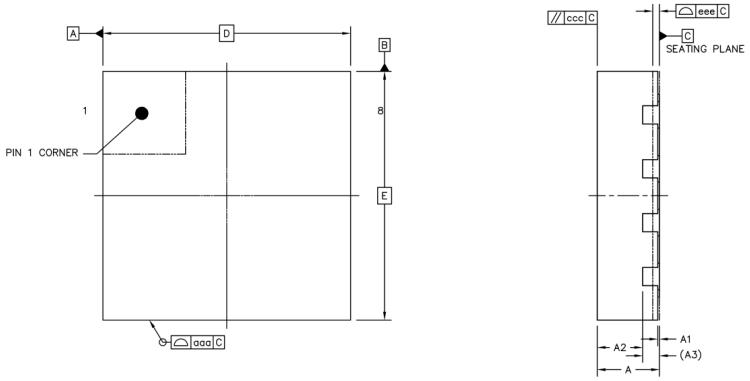






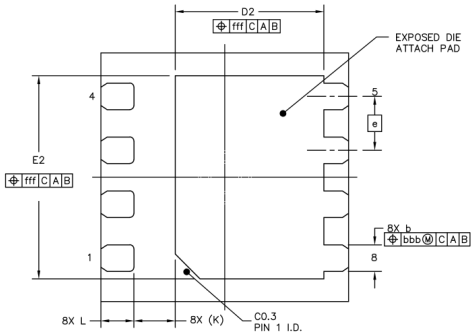


DFN3× 3-8L Package Information



TOP VIEW

SIDE VIEW



BOTTOM VIEW

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A2	0.550TYP		0.022TYP	
A3	0.203REF		0.008REF	
b	0.270	0.370	0.011	0.015
D	3.000BSC		0.118BSC	
E	3.000BSC		0.118BSC	
e	0.650BSC		0.026BSC	
D2	1.700	1.900	0.067	0.075
E2	2.350	2.550	0.093	0.100
L	0.300	0.500	0.012	0.020
K	0.500REF		0.020REF	
aaa	0.100TYP		0.004TYP	
ccc	0.100TYP		0.004TYP	
eee	0.080TYP		0.003TYP	
bbb	0.100TYP		0.004TYP	
fff	0.100TYP		0.004TYP	