GPL6203 Series

Ultra Low Current Consumption 300mA CMOS Voltage Regulators

Product Summary

The GPL6203 series is a group of positive voltage regulators manufactured by CMOS technology, which has the characteristics of high ripple suppression, ultra-low noise and fast transient response. The GPL6203 series adopts low-ESR ceramic capacitor, which reduces the circuit board space required for power application. The GPL6203 series has low static paranoid current and low voltage difference, which can extend the battery life of portable electronic products. Therefore, this series of products are very suitable for the following scenarios: battery powered equipment, wireless communication and industrial equipment, and so on.

GPL6203 provides the package of SOT-23-3L and SOT-23-5L, which is suitable for small equipment and meets the requirements of RoHS and unlead.

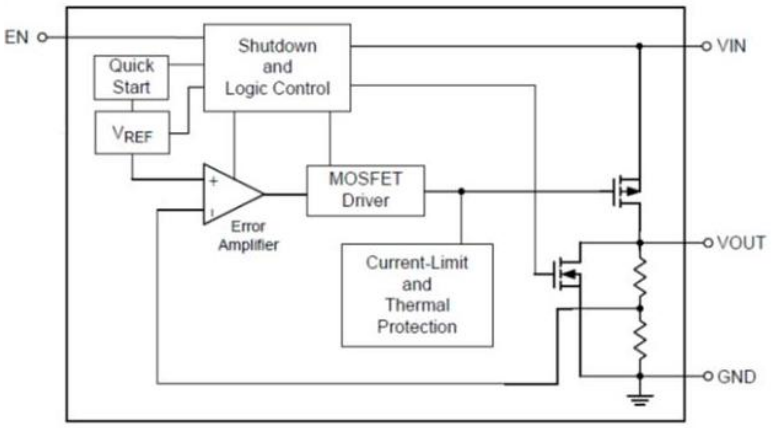
Features

- Low Quiescent Current: 70uA(Typ.)
- Operating Voltage Range: 2V～6V
- Output Current: 300mA
- Low Dropout Voltage:90mV@100mA
- Output Voltage: 1.2~3.6V
- High Accuracy: ±2%(Typ.)
- High Power Supply Rejection Ratio: 70dB@1kHz
- Excellent Line and Load Transient Response
- Built-in Current Limiter, Short-Circuit Protection

Applications

- Portable consumer equipments
- Radio control systems
- Laptop, Palmtops and PDAs
- Wireless Communication Equipments
- Portable Audio Video Equipments
- Ultra-low Power Microcontroller

Block Diagram



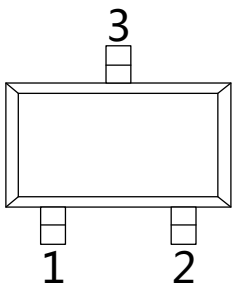
Order Information

GPL6203V①②

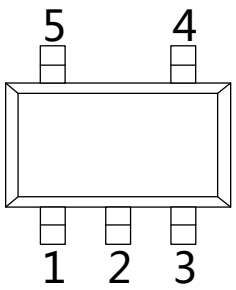
Designator	Description
①	Output Voltage e.g. 1.8V=18
②	Package: SOT-23-3L=K3 SOT-23-5L=K5

Pin Configuration

SOT-23-3



SOT-23-5



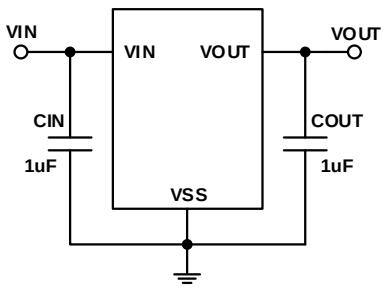
SOT-23-3L

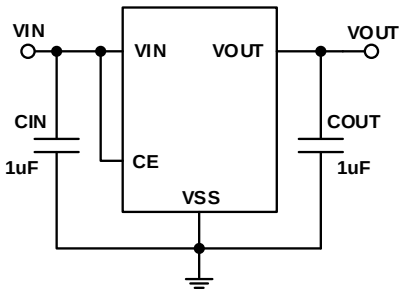
Pin Number			Pin Name	Function
SOT-23-3	TO-92	SOT-89-3L		
1	1	1	V_{SS}	Ground
2	3	3	V_{OUT}	Output
3	2	2	V_{IN}	Power input

SOT-23-5L

Pin Number	Pin Number	Function
1	V_{IN}	Power Input Pin
2	V_{SS}	Ground
3	CE	Chip Enable Pin
4	NC	No Connection
5	V_{OUT}	Output Pin

Typical Application





Absolute Maximum Ratings[1] (T_a=25℃,unless otherwise noted)

Parameter		Symbol	Ratings	Units
Input Voltage[2]		V_{IN}	-0.3~7	V
Output Voltage[2]		V_{OUT}	-0.3~V_{IN}+0.3	V
Output Current		I_{OUT}	300	mA
Power Dissipation	SOT-23-3L	P_D	0.3	W
	SOT-23-5L		0.25	W
Operating Junction Temperature Range		T_j	-40~125	°C
Storage Temperature		T_{stg}	-40~125	°C
Lead Temperature(Soldering, 10 sec)		T_{solder}	260	°C

1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods my affect device reliability.

2) All voltages are with respect to network ground terminal.

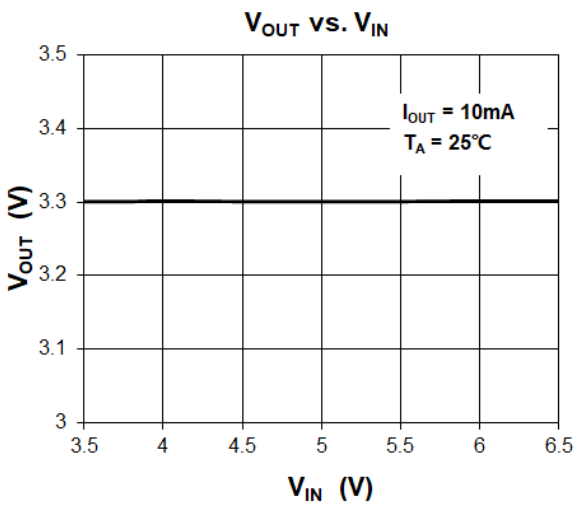
Electrical Characteristics (V_{IN}=V_{OUT}+1V, C_{IN}=C_{OUT}=1μF，T_A=25℃,unless otherwise specified)

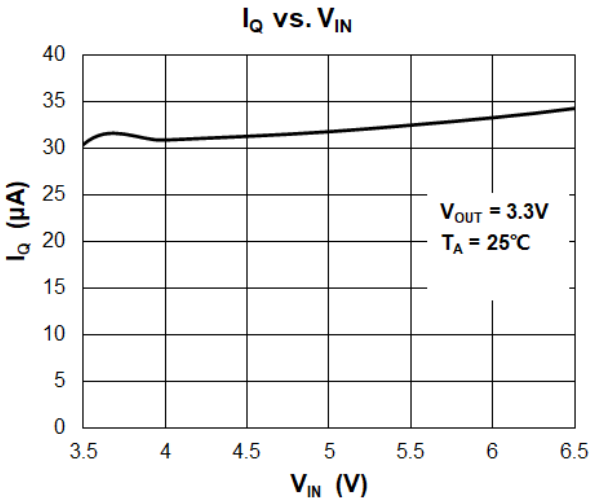
Parameter	Symbol	Conditions		Min.	Typ.[3]	Max.	Units
Input Voltage	V_{IN}					7	V
Output Voltage Range	V_{OUT}			1.2		3.6	V
DC Output Accuracy		I_{OUT}=1mA		-2		2	%
Dropout Voltage	V_{dif}[3]	I_{OUT} =100mA			90		mV
Supply Current	I_{SS}	I_{OUT}=0,V_{IN} = V_{OUT} +1V			70		μA
Standby Current	I_{STBY}	CE=V_{SS}			1		μA
Line Regulation	$\frac{\Delta V_{OUT}}{V_{OUT} \times \Delta V_{IN}}$	I_{OUT} =40mA V_{OUT} +1V≤V_{IN}≤6V			0.05	0.3	%/V
Load Regulation	ΔV_{OUT}	V_{IN}= V_{OUT} +1V, 1mA≤I_{OUT}≤100mA			50		mV
Temperature Coefficient	$\frac{\Delta V_{OUT}}{V_{OUT} \times \Delta T_A}$	I_{OUT}=10mA, -40°C<T_A<125°C			100		ppm
Output Current	I_{OUT}	V_{IN} = V_{OUT} +1V			300		mA
CE Enable Voltage	V_{CE}[4]	V_{IN} = V_{OUT} +1V			1.1		V
Output Noise	en	I_{OUT}=40mA,300Hz~50kHz			50		uVrms
Power Supply Rejection Ratio	PSRR	I_{OUT}=40mA	1kHz		70		dB

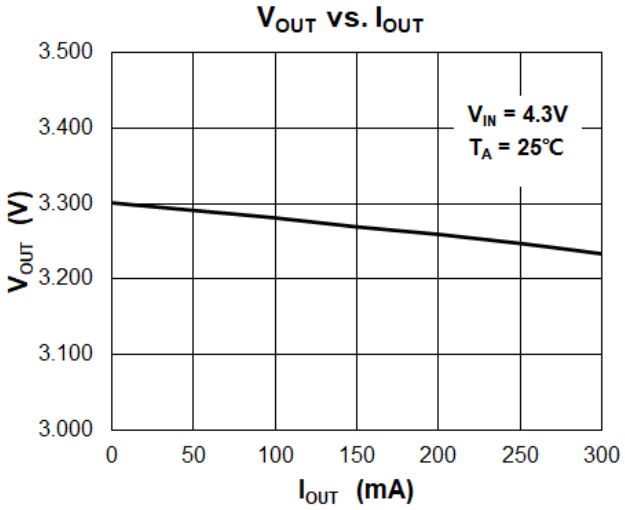
3) The difference of output voltage and input voltage when input voltage is decreased gradually till output voltage equals to 98% of VOUT(E).

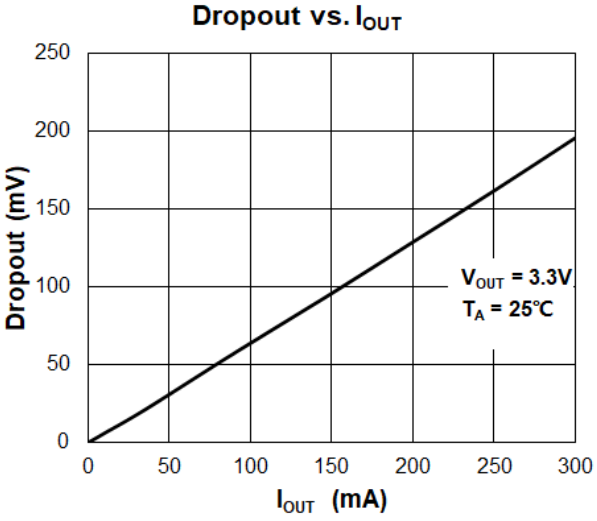
4) Considering the high and low temperature and process devation, it is recommended that the customer set the enable voltage of CE pin (V_{CE}) to 1.1V, with margin. There is a built-in resistance (1MΩ) between CE and GND in the chip.

Typical Performance Characteristics

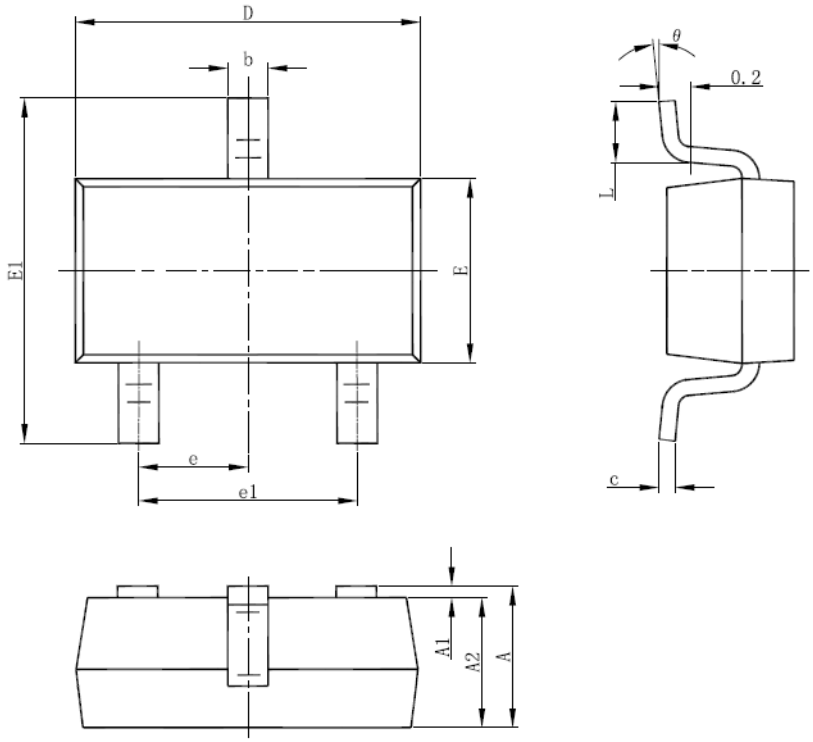






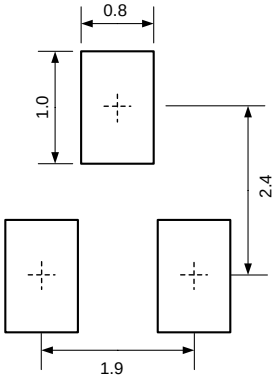


SOT-23-3L Package Outline Dimensions



Symbol	Dimensions in millimeters	
	Min.	Max.
A	1.050	1.250
A1	0.000	0.100
A2	1.050	1.150
b	0.300	0.500
c	0.100	0.200
D	2.820	3.020
E	1.500	1.700
E1	2.650	2.950
e	0.950TYP	
e1	1.800	2.000
L	0.300	0.600
θ	0°	8°

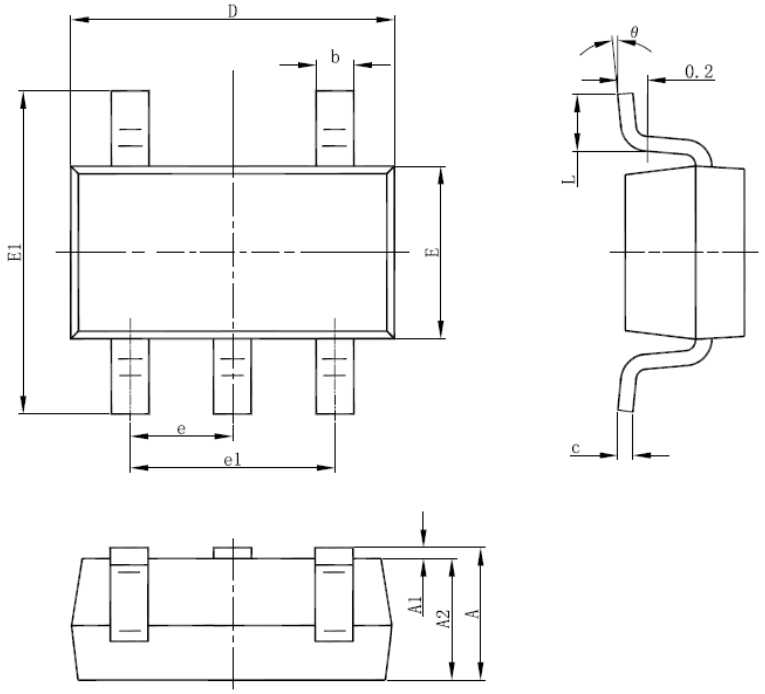
SOT-23-3L Suggested Pad Layout (Unit: mm)



Notes:

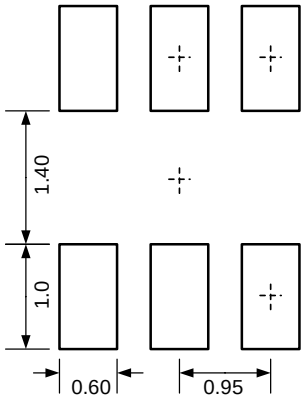
1. General tolerance:±0.05mm.
2. The pad layout is for reference purposes only.

SOT-23-5L Package Outline Dimensions



Symbol	Dimensions In Millimeters	
	Min.	Max.
A	1.050	1.250
A1	0.000	0.100
A2	1.050	1.150
b	0.300	0.500
c	0.100	0.200
D	2.820	3.020
E	1.500	1.700
E1	2.650	2.950
e	0.950(BSC)	
e1	1.800	2.000
L	0.300	0.600
θ	0°	8°

SOT-23-5L Suggested Pad Layout (Unit: mm)



Notes:

1. General tolerance:±0.05mm.
2. The pad layout is for reference purposes only.