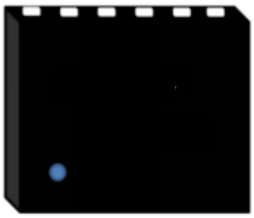
AE-GPFBM75N04FR

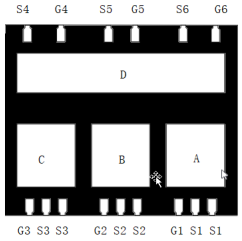
40V Full bridge N-Channel MOSFET

Product Summary

$V_{(BR)DSS}$	$R_{DS(on)TYP}$	I_D
40V	3.9mΩ@10V	75A
	5.0mΩ@4.5V	

DFN14×12-15L





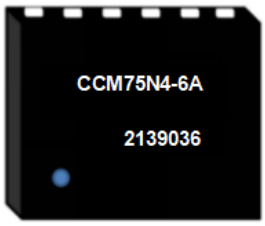
Feature

- Trench Technology
- Low $R_{DS(ON)}$
- Low Gate Charge
- Low Gate Resistance
- 100% UIS Tested
- AEC Q101 qualified

Application

- motor control
- Full bridge module

MARKING:



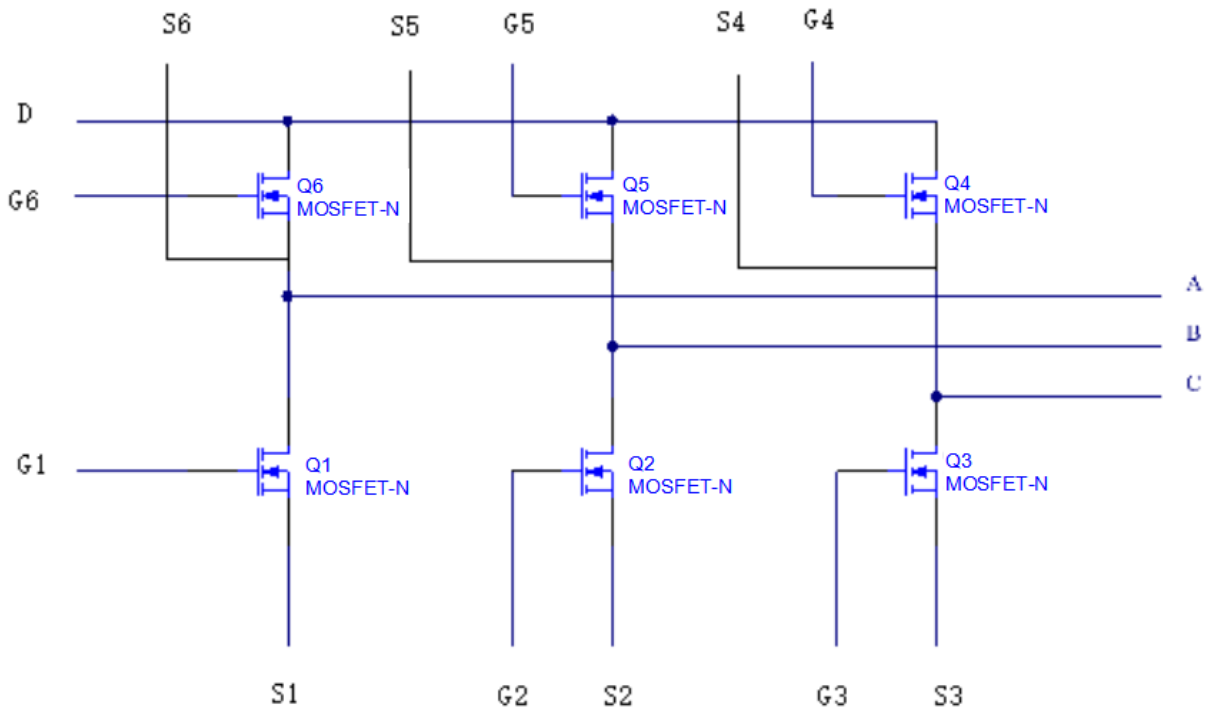
CCM75N4-6A = Device Code

XX = Date Code

ABSOLUTE MAXIMUM RATINGS (T_A = 25℃ unless otherwise noted)

Parameter		Symbol	Value	Unit
Drain - Source Voltage		V_{DS}	40	V
Gate - Source Voltage		V_{GS}	±20	V
Continuous Drain Current[1]	T_C = 25℃	I_D	75	A
Pulsed Drain Current[2]		I_{DM}	300	A
Single Pulsed Avalanche Current[3]		I_{AS}	31	A
Single Pulsed Avalanche Energy[3]		E_{AS}	240	mJ
Power Dissipation[5]	T_C = 25℃	P_D	83	W
Thermal Resistance from Junction to Case[6]		$R_{\theta JC}$	1.8	℃/W
Junction Temperature		T_J	175	℃
Storage Temperature		T_{STG}	-55~ +175	℃

EQUIVALENT CIRCUIT



Number	Pin Definition	Remark	Number	Pin Definition	Remark
1	S1	Lower bridge u phase source	11	G4	Upper bridge w gate
2	S1	Lower bridge u phase source	12	S5	Upper Bridge v phase source collection
3	G1	Lower bridge u phase gate	13	G5	Upper bridge v gate
4	S2	Lower bridge v phase source	14	S6	Upper Bridge u phase source collection
5	S2	Lower bridge v phase source	15	G6	Upper bridge u gate
6	G2	Lower bridge v phase gate	PAD 1	D	DC Input
7	S3	Lower bridge w phase source	PAD 2	A	A phase output
8	S3	Lower bridge w phase source	PAD 3	B	B phase output
9	G3	Lower bridge w phase gate	PAD 4	C	C phase output
10	S4	Upper Bridge w phase source collection			

MOSFET ELECTRICAL CHARACTERISTICS (T_J = 25℃ unless otherwise noted)

Parameter	Symbol	Test Condition	Min	Type	Max	Unit
Off Characteristics						
Drain - Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0V, I_D = 250μA	40			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 40V, V_{GS} = 0V			1	μA
Gate - Body Leakage Current	I_{GSS}	V_{GS} = ±20V, V_{DS} = 0V			±100	nA
On Characteristics[4]						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250μA	1.0	1.7	3.0	V
Drain-source On-resistance	$R_{DS(on)}$	V_{GS} = 10V, I_D = 10A		3.9	6.2	mΩ
		V_{GS} = 4.5V, I_D = 10A		5.0	7.2	
Forward Transconductance	g_{fs}	V_{DS} = 10V, I_D = 10A		70		S
Dynamic Characteristics						
Input Capacitance	C_{iss}	V_{DS} = 25V, V_{GS} = 0V, f = 1MHz		6800		pF
Output Capacitance	C_{oss}			408		
Reverse Transfer Capacitance	C_{rss}			331		
Gate Resistance	R_g	V_{DS} = 0V, V_{GS} = 0V, f = 1MHz		1.5		Ω
Switching Characteristics						
Total Gate Charge	Q_g	V_{DS} = 20V, V_{GS} = 10V, I_D = 20A		31		nC
Gate-source Charge	Q_{gs}			6		
Gate-drain Charge	Q_{gd}			4		
Turn-on Delay Time	$t_{d(on)}$	V_{DD} = 20V, V_{GS} = 10V, R_L = 1Ω, R_G = 3Ω		7		ns
Turn-on Rise Time	t_r			3		
Turn-off Delay Ttime	$t_{d(off)}$			24		
Turn-off Fall Time	t_f			4		
Source - Drain Diode Characteristics						
Diode Forward Voltage[4]	V_{SD}	V_{GS} = 0V, I_S = 10A			1.2	V
Continuous drain-source diode forward Current1	I_S	-			75	A
Pulsed drain-source diode forward current[1]	I_{SM}	-			300	A
Reverse recovery time	T_{rr}	I_F = 10A，dI/dt = 100A/us		26		Ns
Reverse recovery charge	Q_{rr}			28		nC

Notes :

1.The maximum current rating is limited by package.And device mounted on a large heatsink

2.Pulse Test : Pulse Width ≤ 10μs, duty cycle ≤ 1%.

3.E_{AS} condition: V_{DD} = 50V,V_{GS} = 10V, L = 0.5mH, R_G = 25Ω Starting T_J = 25°℃.

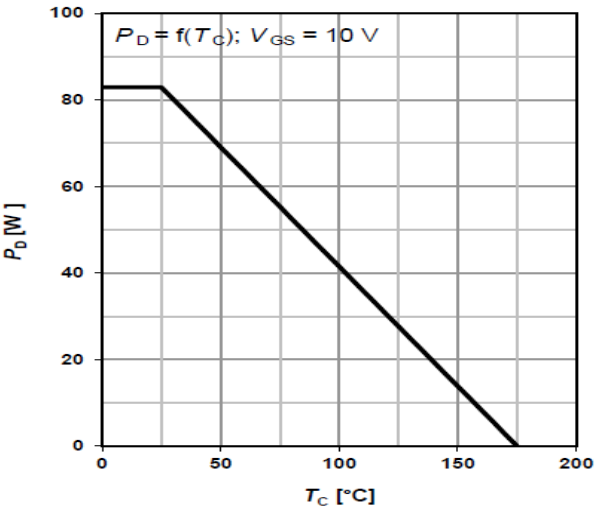
4.Pulse Test : Pulse Width ≤ 300μs, duty cycle ≤ 2%.

5.The power dissipation P_D is limited by $T_{J(MAX)}$ = 150°C.And device mounted on a large heatsink

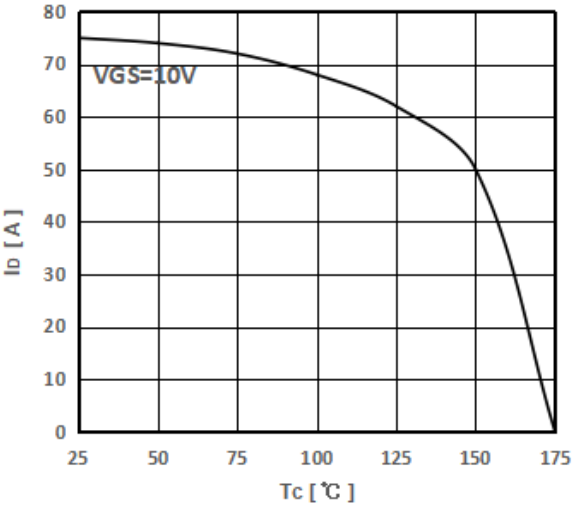
6.Device mounted on 1in^2 FR-4 board with 2oz. Copper, in a still air environment with T_A =25°C.

Typical Characteristics

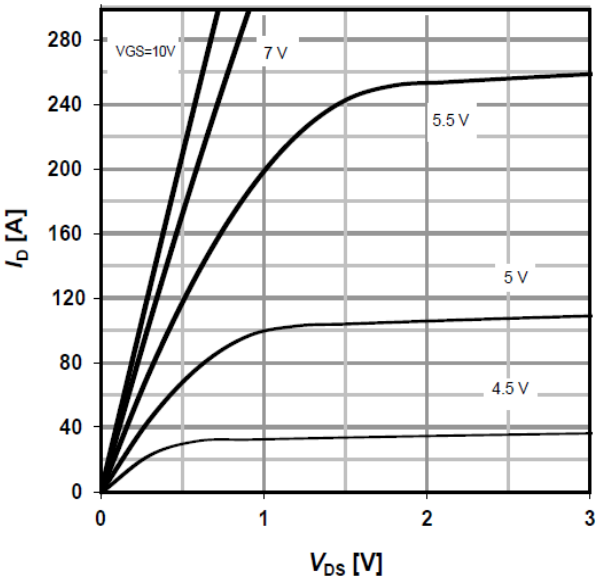
PD vs Tc



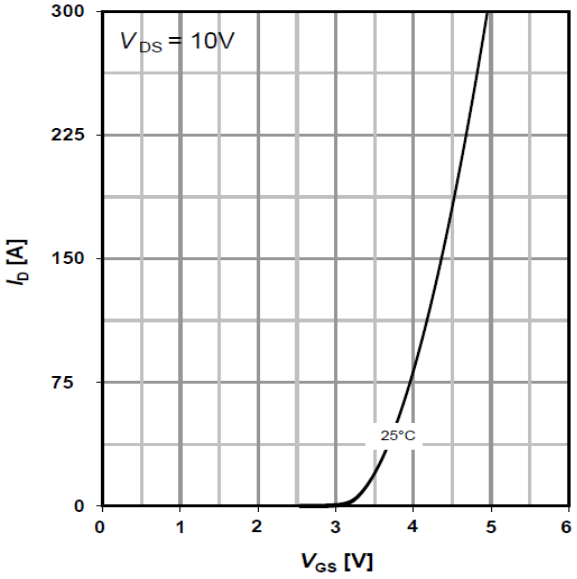
ID vs Tc



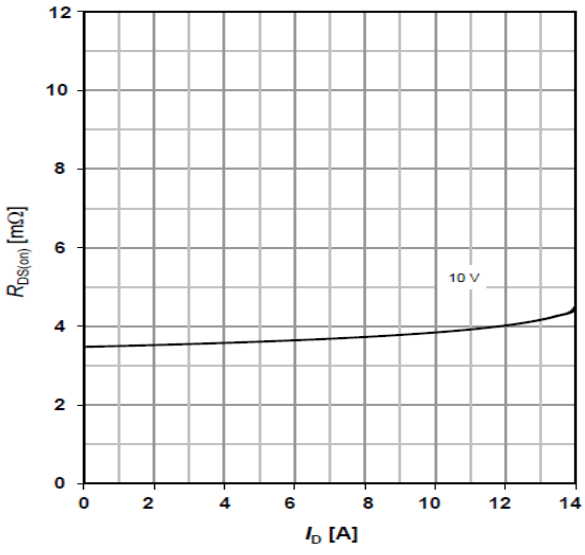
ID vs VDS



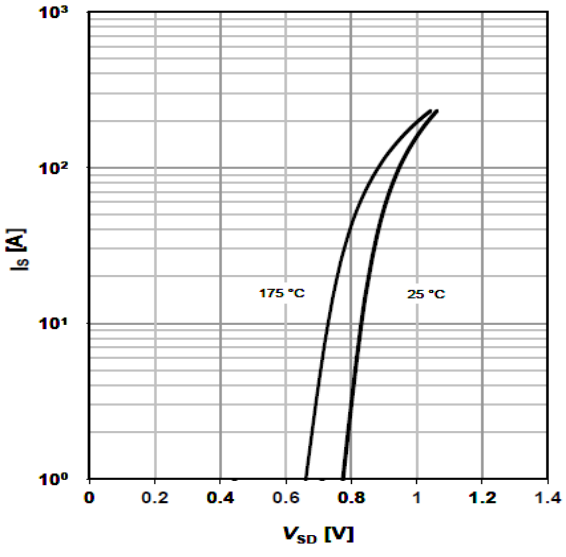
ID vs VGS



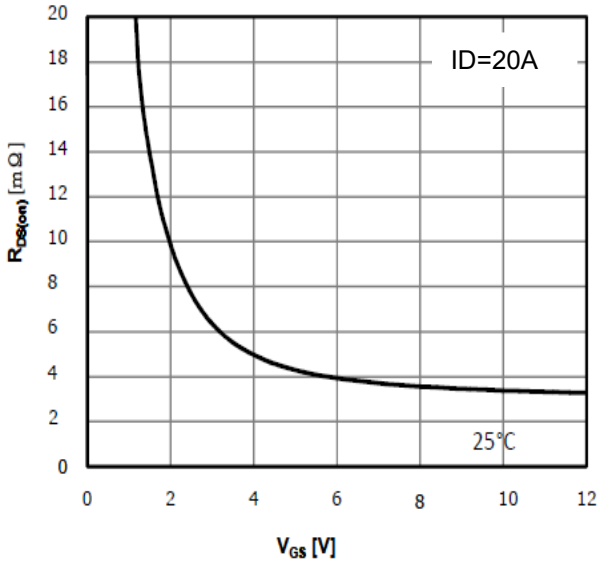
RDS(on) vs ID



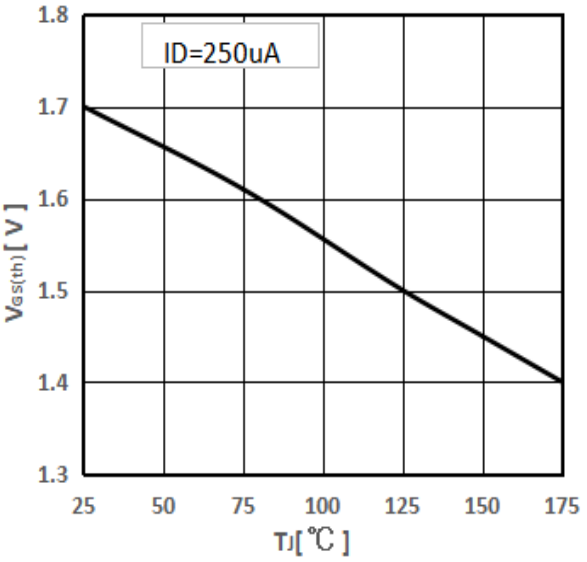
Is vs VSD



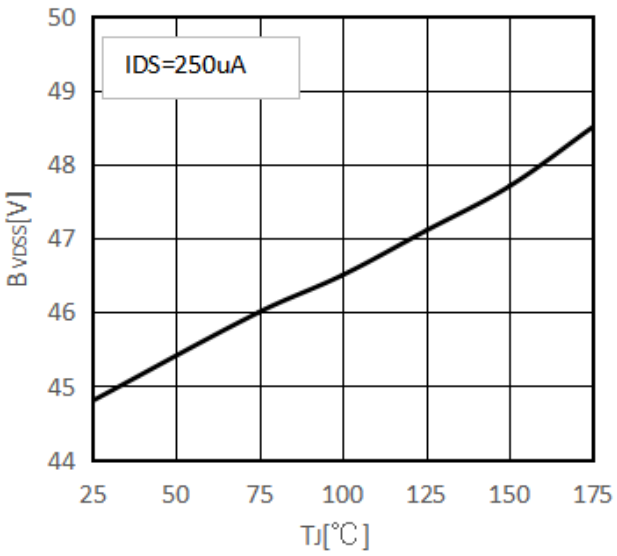
RDS(on) vs VGS



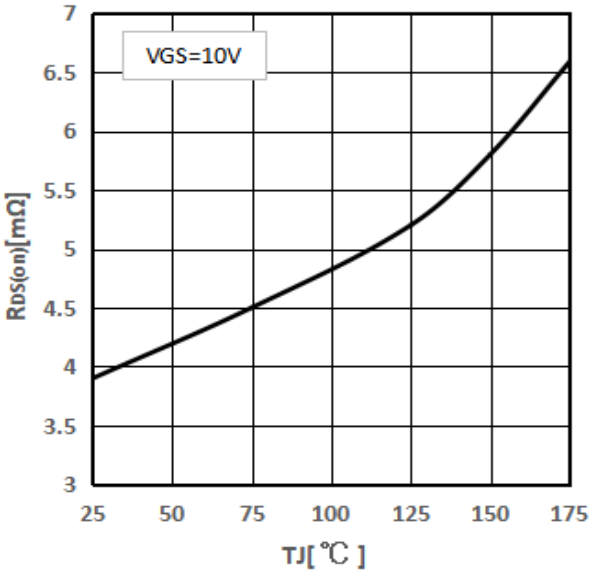
Threshold Voltage



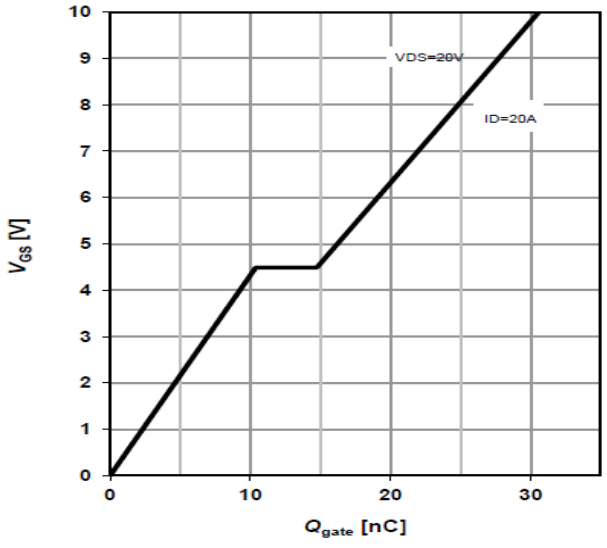
Drain-source breakdown voltage



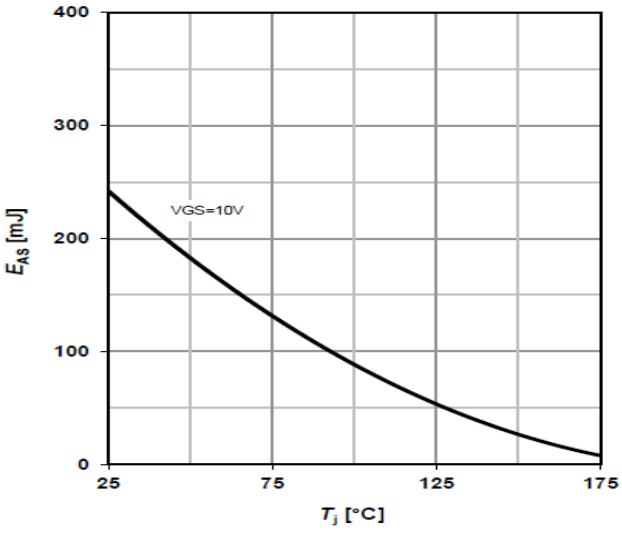
RDS(on) vs TJ



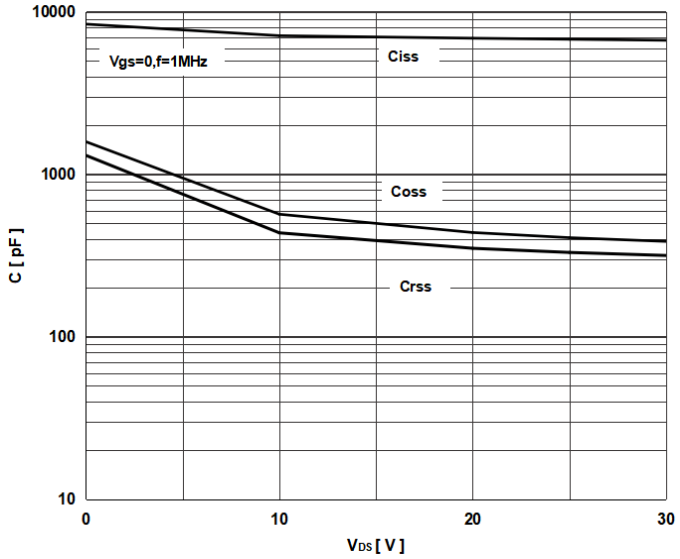
Typ.gate charge



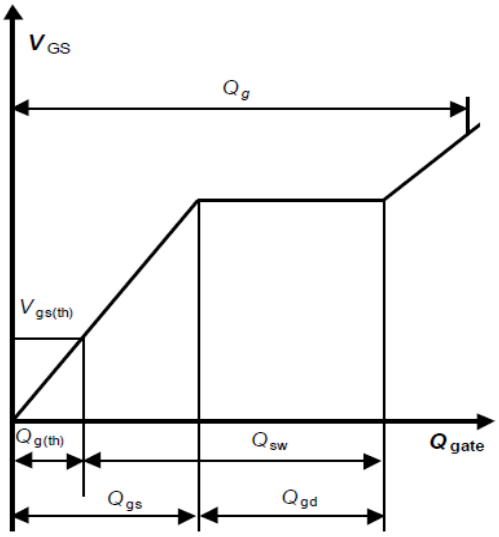
Avalanche energy



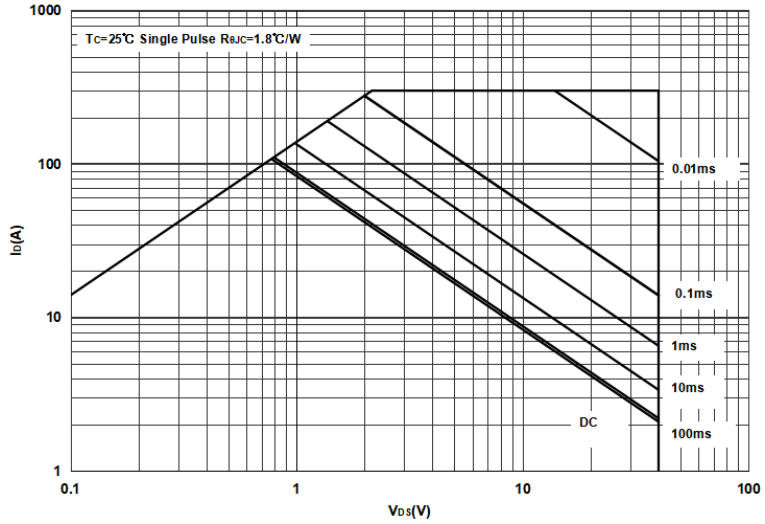
Typ.capacitances



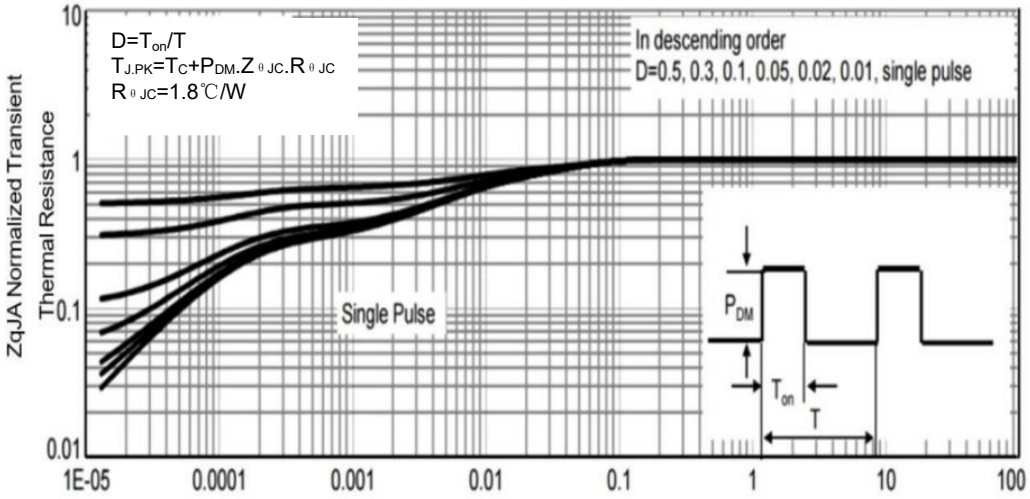
Gate charge waveforms



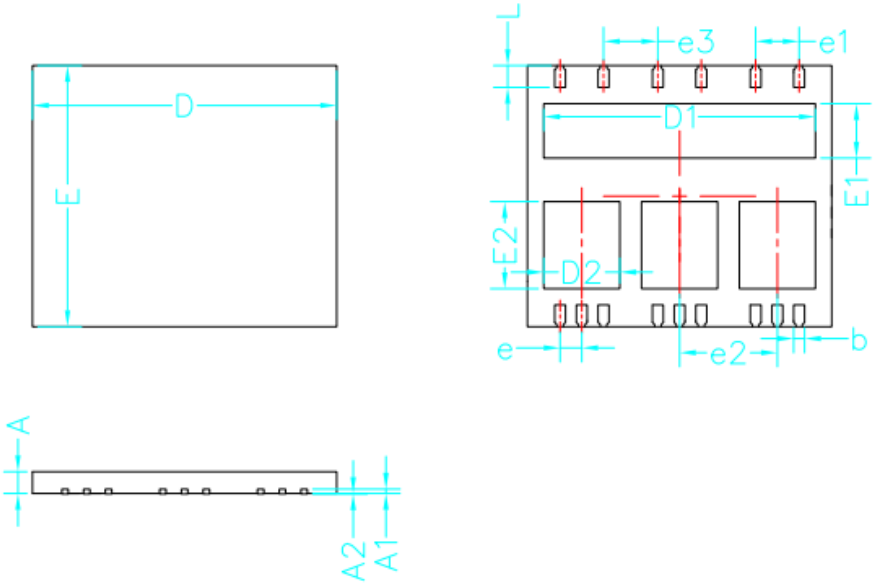
Maximum Forward Biased Safe Operating Area



Normalized Thermal Transient Impedance



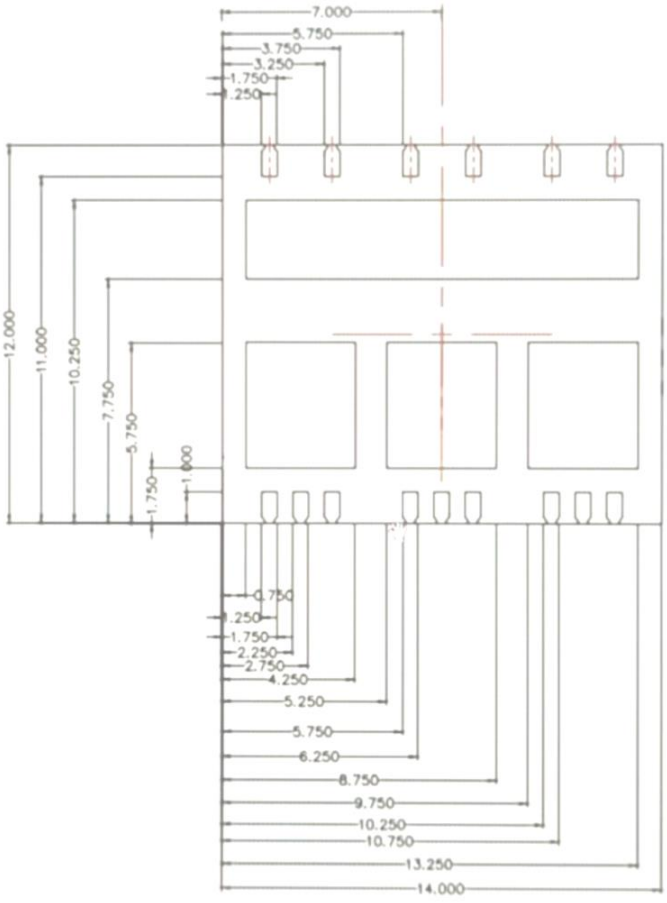
TO-220-3L-C Package Information



unit: mm

	MIN	NOM	MAX
D	13.90	14.00	14.10
E	11.90	12.00	12.10
D1	12.45	12.50	12.55
E1	2.45	2.50	2.55
D2	3.45	3.50	3.55
E2	3.95	4.00	4.05
L	0.95	1.00	1.05
b	0.45	0.50	0.55
e		1.00BSC	
e1		2.00BSC	
e2		4.50BSC	
e3		2.50BSC	
A	0.95	1.00	1.05
A1		0.203REF	
A2	0.00	0.02	0.05

TO-220-3L-C Suggested Pad Layout



Note:
1. Controlling dimension：in millimeters.
2. General tolerance:0.5mm.
3. The pad layout is for reference purposes only.